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Printed Wiring Board Industry and Use Cluster Profile

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Table of Contents

Table of Contents (continued)

PART TWO: USE CLUSTER PROFILE OF THE PWB INDUSTRY (continued)

Table of Contents (continued)

PART TWO: PWB USE CLUSTER PROFILE (continued)

List of Tables

List of Figures

EXECUTIVE SUMMARY

This report presents a profile of the printed wiring board (PWB) industry, and defines and describes the typical manufacturing steps or "use clusters" in the manufacture of multilayer rigid PWBs.

INTRODUCTION

PWBs serve to interconnect the devices and components in the vast majority of electronic products. Without this critical component, most electronic products either could not function or would be significantly more expensive if constructed with other interconnect technologies. PWBs play a crucial role in the advancement of electronic packaging and interconnections because improvements in PWBs reduce the size and cost of electronic devices while boosting performance. Progress in PWB technology and manufacturing drives U.S. competitiveness in both existing products and new technologies. The U.S. Department of Defense (DoD), the U.S. Department of Commerce (DoC), the Japanese Ministry of International Trade and Industry (MITI), and the European Community (EC) all include electronic systems and components on their critical technology lists.

BACKGROUND

A March 1993 report published by MCC (the Microelectronics and Computer Technology Corporation) entitled, Environmental Consciousness: A Strategic Competitiveness Issue for the Electronics and Computer Industry, identified key environmental technology needs in electronics systems manufacturing. The study concluded that effective collaboration between government, industry, academia, and the public is vital for developing and implementing environmentally conscious products and processes. Industry and government programs in environmental technology should encourage such collaboration and focus on specific pilot projects.

The study effort stimulated a collaborative effort to develop a roadmap for the electronics industry. The final roadmap document, released in December of 1994, was produced through a collaborative process that collectively involved more than 100 organizations, including the Advanced Research Projects Agency (ARPA), DoE and the Environmental Protection Agency (EPA), and several prominent trade associations. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) was instrumental in developing the information on PWBs through its Environment, Health, and Safety Committee. The EPA Design for the Environment PWB Project was stimulated in part by both of these activities.

DESIGN FOR THE ENVIRONMENT PROJECT

This profile report was prepared in support of the U.S. EPA Design for the Environment PWB Project. The Project is a cooperative effort between the EPA, IPC, MCC, industry, research institutions, and public interest stakeholders to identify and assess environmentally safer substitute materials, processes, and technologies for the PWB industry. This report—a profile of the industry (Part 1) and description of the major industry processes (Part 2)—is one step in the overall assessment. The information contained in this report contributes to the selection of specific materials, processes, and technologies to be investigated further.

PART 1: INDUSTRY PROFILE

The total world market for all PWBs is approximately $21 billion, of which U.S. production accounts for about one quarter (>$5 billion). U.S. domination of this world market eroded from 1980 to

1990, but has come back slightly in recent years. However, like a commodity industry, the PWB industry is characterized by highly competitive global sourcing with very low profit margins.

There are approximately 700 to 750 independent PWB manufacturing facilities in the U.S. In addition, there are approximately 70 captive printed wiring board facilities. The states with the highest number of PWB manufacturing facilities are California, Minnesota, Texas, Illinois, Massachusetts, and Arizona. However, there are PWB manufacturing facilities in virtually all 50 states and territories. In sheer numbers, the vast majority of PWB manufacturers are small to medium enterprises with annual sales under $10 million. In the U.S., the majority of PWBs (>75%) are produced by independent manufacturers. Many original equipment manufacturers (OEMs) have shut down their PWB operations and now buy their PWBs from independent manufacturers.

Since 1980, rigid multilayer PWBs have grown to dominate the domestic production value of all PWBs. Rigid multilayer boards now account for approximately 66% of the domestic market. One-quarter of the market is double-sided rigid boards, and the remainder are single-sided and flexible circuits. The market for multilayer boards has grown from approximately $700 million in 1980, to almost $3.4 billion in 1993. The PWB industry directly employs approximately 75,000 people. Of this number, about 68% of employment is concentrated in production jobs—the highest ratio of production jobs for U.S. electronic manufacturing.

IPC estimates that a minimum of 2% of PWB revenues in 1991 went to pay for pollution controls. In comparison, the average net profit for the PWB industry in 1991 was about 2.2% of sales. The cost of waste treatment (estimated at over $140 million in 1990 for major merchant PWB manufacturers) and the additional regulatory burdens of recordkeeping, manifesting, and inventory reporting constitute a significant cost to the PWB manufacturers in this country. The fundamental processes, however, have remained the same and many pollution prevention efforts have reached their cost-effective limits. Part 2 of this document will describe the PWB manufacturing process and identify alternative technologies that may be evaluated in a design for the environment effort, thereby decreasing cost and environmental impact simultaneously.

PART 2: USE CLUSTER PROFILE

PWB manufacturing is a highly technical, complicated operation requiring large equipment investments and over fifty processes. The manufacturing processes described in Part 2 are organized and described in "use clusters." A use cluster is a set of chemicals, processes, and technologies that can substitute for one another to perform a specific function. A use cluster profile of the industry, therefore, describes alternate chemicals, processes, or technologies that may be used to complete each step or function in the entire PWB manufacturing process.

This PWB use-cluster profile describes the fabrication processes for the largest product segment of the industry, the rigid multilayer PWB. The use cluster profile is intended to aid in the selection of a use cluster for assessment in a DfE project. The profile identifies different processes in the PWB industry (e.g., laminating, making holes conductive) and steps within those processes (e.g., imaging, etching, plating). The process steps are described in flow chart form with a description of each step. Next, the chemicals, processes, and technologies used in each step are briefly described. The profile may also mention commonly accepted alternatives to these practices and areas that are recognized to have especially high environmental impacts. Information on the risk and releases of these materials can then be investigated to target areas for further work but is not within the scope of this report.

PART ONE:

PWB INDUSTRY PROFILE

I. INTRODUCTION AND OVERVIEW

This industry profile refers to the printed wiring board (PWB) industry, SIC 3672.

A. What is a PWB?

A printed wiring board (PWB) is the foundation—both literally and figuratively—for virtually all electronics in the world. It is the platform upon which electronic components such as integrated circuit chips and capacitors are mounted. The PWB, or printed circuit board (PCB) provides both the physical structure for mounting and holding electronic components as well as the electrical interconnection between components. A PWB consists of a non-conducting substrate (typically fiberglass with epoxy resin) upon which a conductive pattern or circuitry is formed. Copper is the most prevalent conductor, although nickel, silver, tin, tin-lead, and gold may also be used as etch-resists or top-level metal. There are three types of PWBs: single-sided, double-sided, and multilayer. Single-sided boards have a conductive pattern on one side only, double-sided boards have conductive patterns on both faces, and multilayer boards consist of alternating layers of conductor and insulating material bonded together. The conductive layers are connected by plated through-holes, which are also used to mount and electrically connect components. PWBs may also be either rigid, flexible, or a combination of the two (rigid-flex).

When the electronic components have been mounted on the PWB, the combination of PWB and components is an electronic assembly, also called a printed wiring assembly (PWA). This assembly is the basic building block for all larger electronic systems, from toys to toasters to telecommunications.

These electronic systems, in turn, support every other critical technology in the United States. To quote the Council on Competitiveness from their 1991 Gaining New Ground report, "Electronic components are playing an especially important role in driving improvements in information and communication technologies, which in turn are enabling advances in all manufacturing and service industries."

PWBs play a crucial role in these improvements because advances in electronic packaging and interconnections reduce the size and cost of electronic devices while boosting performance. Progress in PWB technology and manufacturing drives U.S. competitiveness in both existing products and new technologies. The U.S. Department of Defense, the U.S. Department of Commerce, the Japanese Ministry of International Trade and Industry, and the European Community all include electronic systems and components on their critical technology lists.

Electronics drive productivity in almost every industry—one electronics job determines the competitive strength of seven jobs in other industries. Electronics are critical in medical systems, defense technologies, information processing, intelligent manufacturing, propulsion, and materials processing. In addition, a number of new, emerging industries depend on advancing the technical capability of the PWB industry. These include artificial intelligence, biotechnology, digital imaging technology, high-density data storage, high-performance computing, medical devices and diagnostics, opto-electronics, and more. U.S. competitiveness in these new technologies will depend upon advanced PWB technology and manufacturing capability in the United States.

B. Independent vs. Captive Production

PWBs are produced by two types of manufacturers: independent and captive. An independent or merchant manufacturer produces PWBs for sale on the open market, to be used in electronic products such as TVs, computers, and so forth. Independent PWB manufacturers are thus competing

with each other in a global market to secure orders or contracts from customers. Typically, independent PWB manufacturers bid on their ability to make a product as specified by the customer; the PWBs or electronic interconnection products are almost always custom designed.

A captive manufacturer is also known as an Original Equipment Manufacturer or OEM. These companies manufacture PWBs for use internally in their own electronic products. Texas Instruments and AT&T are examples of OEMs. Some OEMs, such as IBM, which in the past have been exclusively captive manufacturers, have recently entered the merchant market as well.

In the United States, the majority of PWBs are produced by independent manufacturers. Many OEMs have shut down their PWB operations and now buy their PWBs from independent manufacturers. Unfortunately, as OEMs shut down their PWB manufacturing, they also discontinue research and development on new PWB manufacturing technology, processes, and materials. Because the average independent PWB manufacturer is orders-of-magnitude smaller than most OEMs, the independent PWB manufacturer lacks sufficient resources to conduct research on any scale approaching what the OEMs used to accomplish. Thus, PWB technology development in the United States has slowed down considerably.

C. General Nature of Industry

PWB manufacturing is a highly technical, complicated operation requiring large equipment investments and over fifty process steps. Because PWBs are designed for individual, specific applications, the PWB manufacturing industry is not considered a commodity industry. However, like a commodity industry, the PWB industry is characterized by highly competitive global sourcing with very low profit margins. Designs for specific PWBs can be transmitted electronically virtually anywhere in the world for fabrication.

In the United States, unlike some other areas of the world, the PWB industry has made substantial investments in pollution prevention and control, and is continuing to spend an average of 2.1% and as much as five percent of sales on regulatory compliance and pollution prevention. These investments have paid off with significant pollution prevention successes. For example, the Institute for Interconnecting and Packaging Electronic Circuits (IPC) and several IPC members won EPA Stratospheric Ozone Protection Awards for research on eliminating ozone-depleting substances from PWB manufacturing and assembly. Several IPC members have also won EPA 33/50 Pollution Prevention Awards for their aggressive work on preventing pollution, and many IPC members have won state or local awards for their proactive pollution reduction efforts.

II. COMPANIES AND FACILITIES

A. Number of Companies and Facilities

There are approximately 700 to 750 independent PWB manufacturing facilities in the U.S. In addition, there are approximately 70 captive printed wiring board facilities. The geographic distribution is shown in Table 1-1. The states with the highest PWB manufacturing are California, Minnesota, Texas, Illinois, Massachusetts, and Arizona. However, there are PWB manufacturing facilities in virtually all 50 states and territories.

Region Description		# of PWB Facilities	
Area	States	Captive	Independent
New England	VT, NH, MA, CT, ME, RI	9	65
Mid-Atlantic	PA, NY, NJ	6	68
South Atlantic	VA, WV, MD, DE, NC, SC	6	26
Southeast	TN, MS, AL, GA, FL, PR	7	49
South Central	TX, OK, AR, LA	6	45
Mid-Central	IL, KS, MO, NE	4	53
North Central	MT, ND, SD, MN, IA, WI	8	62
East Central	MI, IN, OH, KY	5	48
Mountain States	WY, CO, UT, NV, AZ, NM	7	43
Northwest	OR, WA, AK, HI	4	21
No. California		0	85
So. California		6	134
Canada	AB, MB, ON, QU, BC, SA	2	48
	Total	**70**	**747**

Source: Kirk-Miller Associates, 1994.

Table 1-1. Distribution of PWB Manufacturing Facilities, 1994.

B. Size of Companies

In sheer numbers, the vast majority of PWB manufacturers are small to medium enterprises with annual sales under $10 million. The breakdown of the number of companies by size is shown in Table 1-2. These numerous smaller companies control only about 20% to 25% of the market dollar volume, while the largest 40 or so companies with annual sales over $20 million control about 55% of the dollar volume of the PWB market. A breakdown of market share by size of company is shown in Figure 1-1.

The PWB industry directly employs approximately 75,000 people. Of this number, about 68% of employment is concentrated in production jobs—the highest ratio of production jobs for U.S. electronic manufacturing. Approximately 50% is the average for other electronic sectors. These employment figures do not include jobs generated by the related PWB material and equipment suppliers of the industry, nor the OEMs that produce PWBs for internal use.

Annual Sales	Number of Companies	Average Shipments per Company	Total Shipments
Over $50 Million	14	$95	$1,330
$20 to $50 Million	30	$31	$1,116
$10 to $20 Million	40	$14	$672
$5 to $10 Million	85	$7	$595
Under $5 Million	500 or more	$<1	$349
Totals	**Over 650**		**$4,062**

Source: IPC Technology Marketing Research Council, June 1994.

Table 1-2. U.S. Independent PWB Manufacturers: Number and Size of Company by Sales (all dollars are in millions).

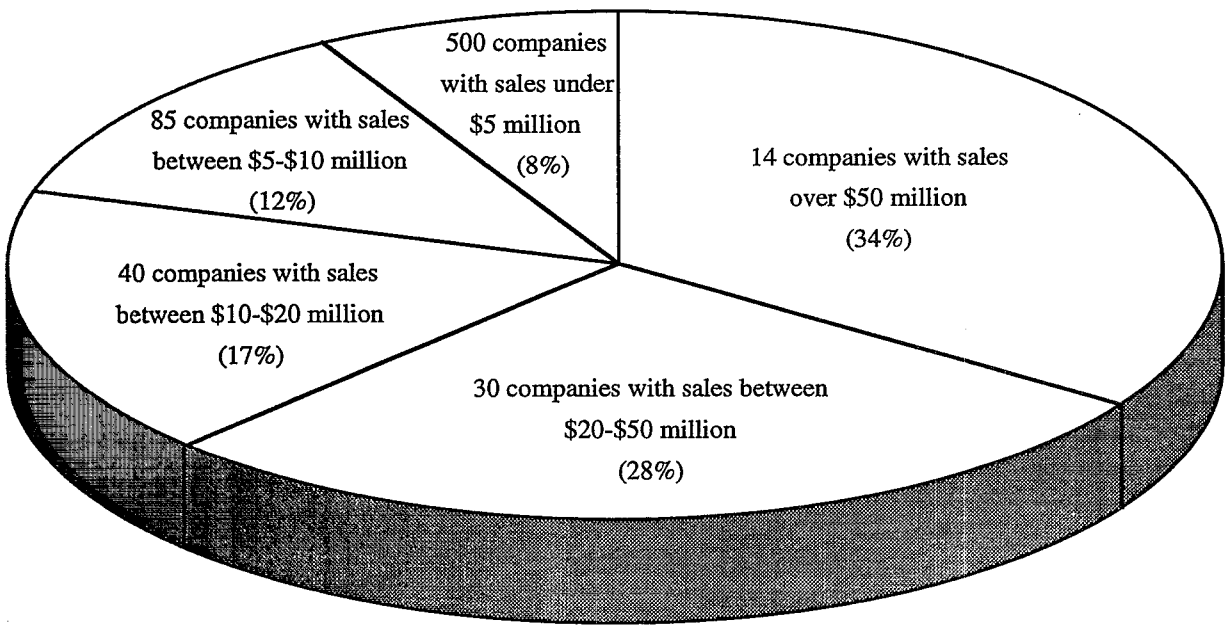

Figure 1-1. U.S. Independent PWB Manufacturers: Market Share by Size of Company. Source: IPC Technology Marketing Research Council, June 1994.

III. FINANCIAL ANALYSIS OF INDUSTRY

Printed wiring board manufacturing is a highly competitive global industry. Although PWBs are not a commodity item, many of the competitive pressures and sourcing patterns are typical of a commodity market.

A. Profitability

Profitability in the industry varies from year to year, but generally falls in the range from 0 to 3%. Extremely stiff foreign competition and adequate global capacity keep the profit range narrow. The net profit after taxes for the domestic PWB industry in 1992 was 1.6%, and in 1993 was 2.9%. While these trends vary annually, in general the largest companies outperform the smallest in terms of profitability, while the mid-size companies fluctuate more between extremes. The reasons for this trend are not entirely clear, but as PWB manufacturing becomes more expensive and capital-intensive, the largest companies may benefit from greater resources and economies of scale.

B. Operating and Financial Ratios

With respect to operating and financial ratios, the following is a summary of typical figures for the industry:

- Pre-tax return on assets: 3% to 5%
- Net sales per employee: $60,000 to $110,000

IV. MARKET ANALYSIS OF INDUSTRY

A. World Market Summary

The total world market for all PWBs is approximately $21 billion.[1] The United States and Japan are the dominant leaders, although the four tigers (Hong Kong, Singapore, Taiwan, and Korea) have been increasing market share in recent years. The distribution of production for rigid PWBs by selected countries and regions is shown in Figure 1-2. The breakdown of the world market for rigid PWBs by type of substrate is shown in Figure 1-3 and, as can be seen, multilayer boards dominate the world market.

A historical perspective on the world market share (in U.S. dollars) for PWBs is shown in Figure 1-4. U.S. domination of this world market eroded from 1980 to 1990, but has come back slightly in recent years. Japan and the four tigers have been the predominant competitors who have captured the world market share lost by the United States. Japan is now seeing its own market dominance erode as the four tigers continue to capture market share.

B. Domestic Market History/Overview

Since 1980, rigid multilayer PWBs have grown to dominate the domestic production value of all PWBs. Rigid multilayer boards now account for approximately 66% of the domestic market. One-quarter of the market is double-sided rigid boards, and the remainder are single-sided and flexible circuits. The market for multilayer boards has grown from approximately $700 million in 1980, to almost $3.4 billion in 1993. Figure 1-5 shows the history of this growth in the multilayer market.

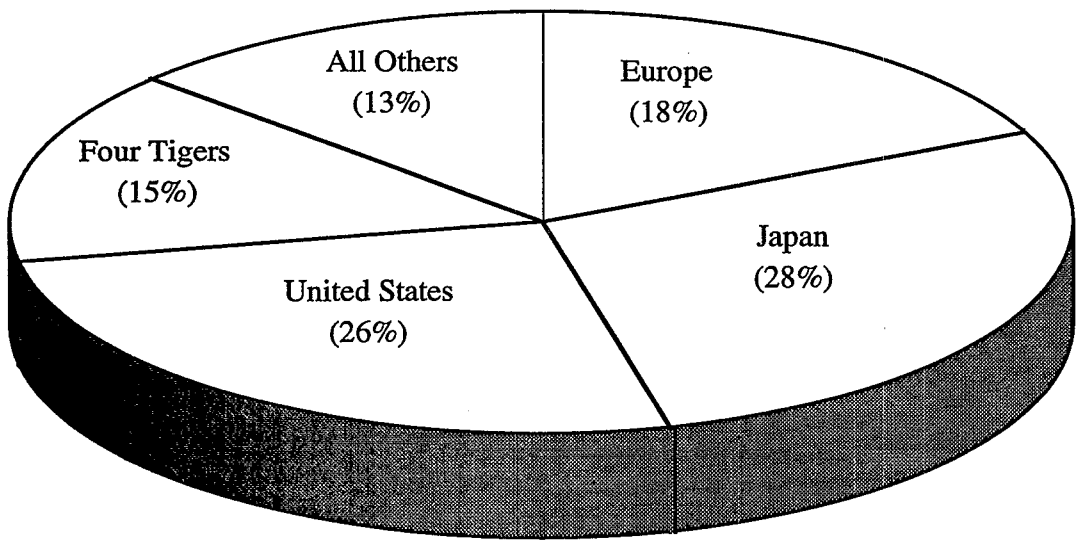

Figure 1-2. U.S. Dollar Denominated[1] Share of World Rigid PWB Market for Selected Countries/Regions. Source: IPC Technology Marketing Research Council, June 1994.

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1 Exchange rates play a major factor in analyzing the world market. Growth and market share depend on which currency is used to measure the markets and the current exchange rate . All world market data in this report are measured in U.S. dollars based upon the exchange rate as of 31 December 1993.

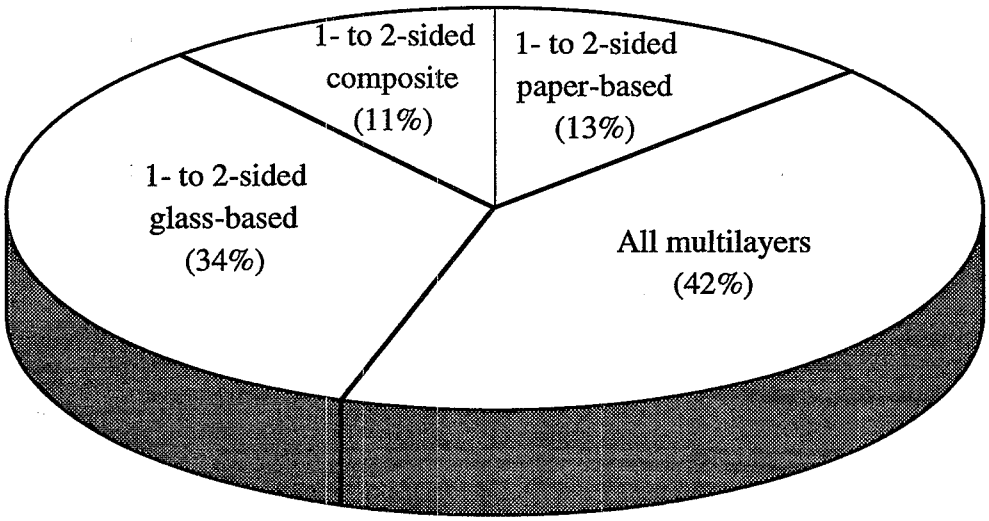

Figure 1-3. U.S. Dollar Denominated[1] Production of World Rigid PWB Market by Type of Substrate.

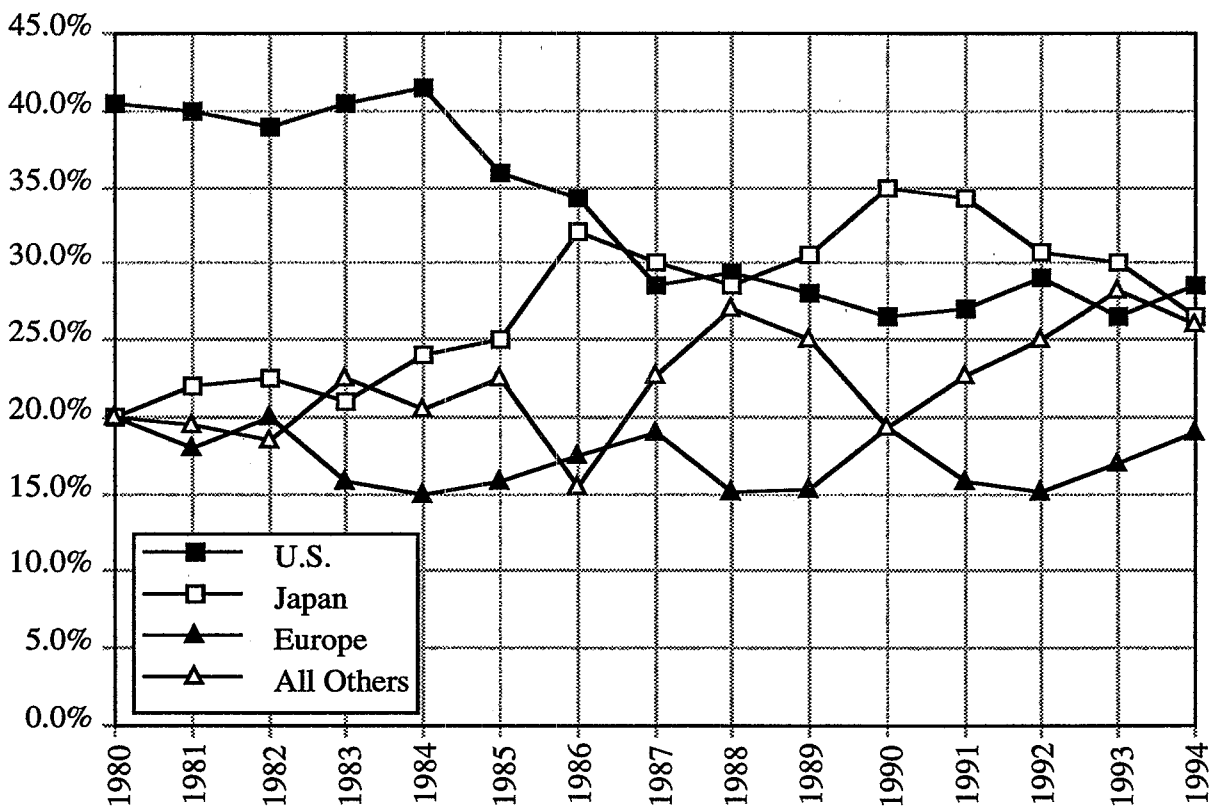

Figure 1-4. Historical World Market Share for Rigid and Flexible Circuits (based on U.S. dollars).[1]

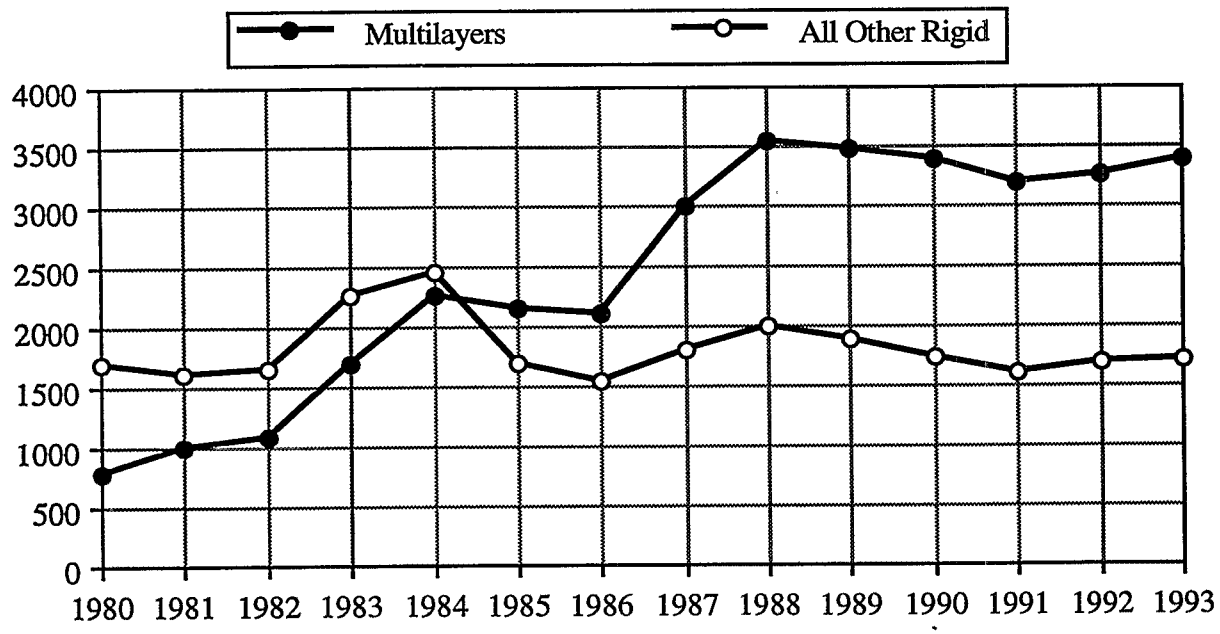

Figure 1-5. Comparison: Multilayers (including high-performance multilayers) vs. All Other Rigid PWBs (excluding flex). All Dollars in Millions.
Source: IPC Technology Marketing Research Council, June 1994.

Although multilayer rigid boards dominate the dollar volume of production, single-sided PWBs by far dominate the number of circuit boards produced in the United States. Of the approximately 1.3 million PWBs produced in the United States in 1993, almost 900,000 were single-sided and only 150,000 were multilayer boards. However, the average cost for a single-sided board is 58¢, while the average cost for a multilayer board is about $22 (Table 1-3).

Another historical shift over the past ten years has been outsourcing PWB manufacturing. In 1980, captive OEM operations accounted for about 50% of the PWB market. Independent or merchant PWB manufacturers accounted for the other half. As is clear from Figure 1-6, captive houses have been shutting down their PWB manufacturing operations and instead purchasing PWBs from the smaller independent manufacturers.

Type of PWB	Total Value of Production	Average Cost per Board	No. of PWBs (in millions)
Multilayer	$3.350 billion	$21.74	154,000
Double-sided	$1.186 billion	$5.65	210,000
Single-sided	$0.521 billion	$0.58	890,000
Totals	$5.057 billion		1,254,000

Source: IPC Technology Marketing Research Council, June 1994

Table 1-3. Quantity and Value of Domestic PWB Production.

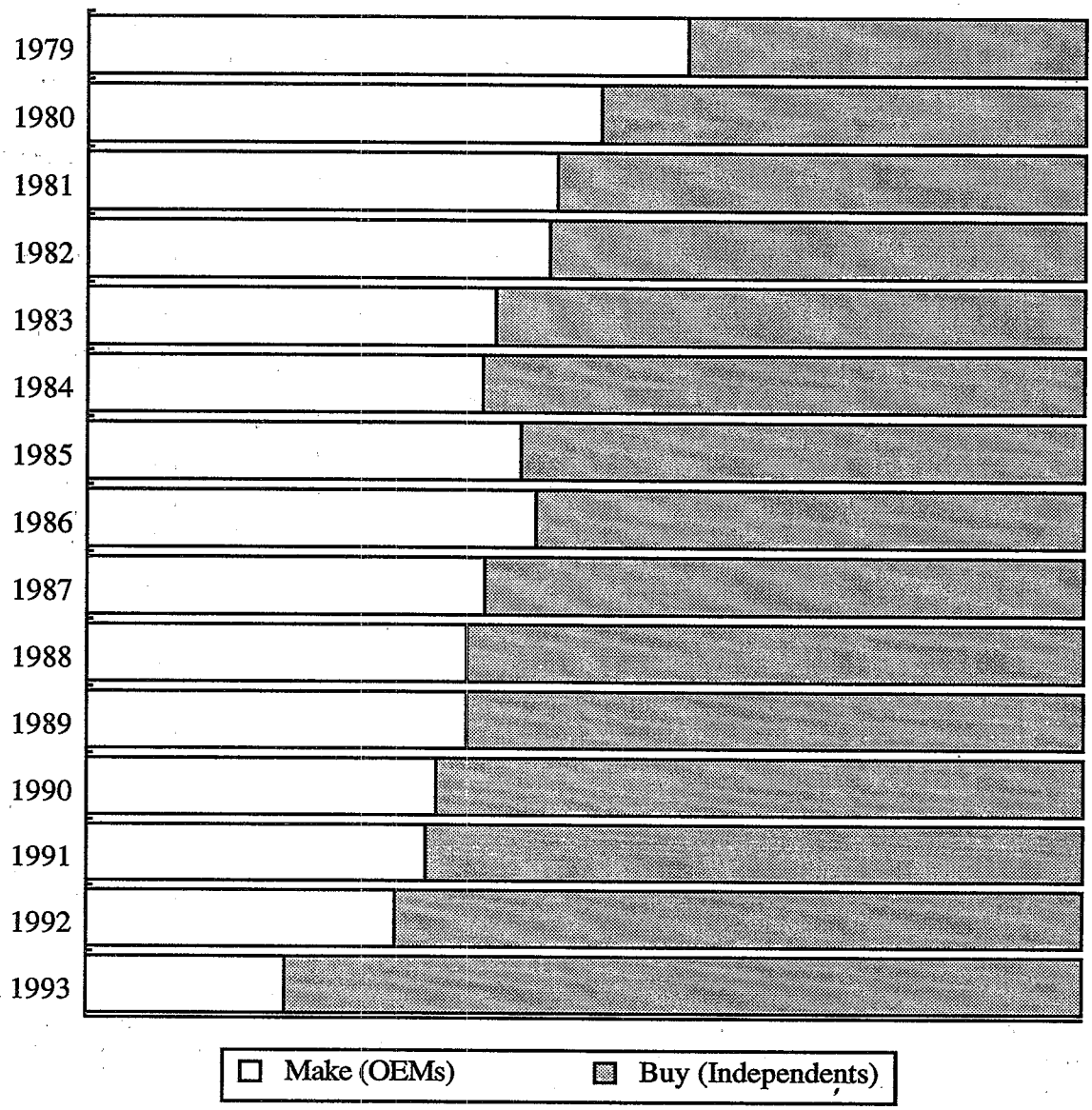

Figure 1-6. Historic Trends of Make vs. Buy for PWB Production in the U.S. (by dollar volume). Source: IPC Technology Marketing Research Council, June 1994.

Now, only one quarter or less of the PWB manufacturing is done by captive houses. The remaining 75% to 80% is produced by independent PWB manufacturers. The reason for this shift is that OEMs are focusing on their core business—assembling the final consumer products—rather than manufacturing all the intermediate components such as PWBs or cathode ray tubes (CRTs). Thus, the OEMs now frequently purchase components (including PWBs, CRTs, subassemblies, drives, etc.) that can be readily out-sourced. Boards are purchased from independent PWB manufacturers who specialize only in PWB production, rather than try to maintain the hefty costs, expensive equipment, personnel, and technical expertise required for in-house PWB production. The introduction of computer-

aided design (CAD) has also facilitated the transfer of design information, and therefore, the outside manufacture of PWBs.

C. Imports/Exports

Import and export data on the PWB market is extremely difficult to estimate, primarily because the nomenclature and codes used by the International Trade Commission and the U.S. Department of Commerce are confused by printed wiring assembly and printed wiring board importers and exporters. Printed wiring assemblies are printed wiring boards on which electronic components such as integrated circuits, capacitors, and resistors have been mounted. With such valuable components mounted on them, the value of PWAs are clearly much greater than bare PWBs.

By combining the U.S. Department of Commerce data with their market research, the IPC estimates that domestic PWB imports are approximately $500 to $600 million annually. The largest single importer is Taiwan with about 30% to 35% of the import market. Japan, Hong Kong, Korea, and Thailand each have about 10% of the import market. With respect to exports, it is estimated that total domestic PWB exports amounted to about $100 million dollars in 1993 (2% to 3% of total domestic production). This estimate does not include PWBs exported by OEMs in their equipment.

D. Major Domestic Markets and Trends

The seven basic markets for printed wiring boards are described below.

- Automotive: engine and drive performance, convenience and safety, entertainment (radios), and other applications for diagnostic display and security.
- Communication: mobile radio, touch tone, portable communication, pagers, data transmissions, microwave relay, telecommunications and telephone switching equipment, and navigation instruments.
- Consumer electronics: watches, clocks, portable calculators, musical instruments, electronic games, large appliances, microwave ovens, pinball/arcade games, television, home entertainment, video records, and smoke and intrusion detection systems.
- Computer/business equipment: mainframe computers, mini computers, broad level processors, add-on memory, input/output devices, terminals, printers, copy machines, facsimile machines, word processors, cash registers, teaching machines, gas pumps, and taxi meters.
- Government/military/aerospace: radar, guidance and control systems, communication and navigation, electronic warfare, ground support, sonar ordinance, missiles, and satellite and related systems.
- Industrial electronics: machine and process control, production test and measurement, material handling, machining equipment, pollution, energy and safety equipment, numerical controls, power controls, sensors, and weighing equipment.
- Instrumentation: test and measurement equipment, medical instruments and medical testers, analytical, nuclear, lasers, scientific instruments, and implant devices.

A summary of the market share for these various groups is shown in Figure 1-7. By far the largest market is computers and business equipment, followed by communications and automotive. Automobiles will use increasing amounts of electronics, and communications demand will continue strong growth. Computer and business equipment may be leveling off, while government and military electronic demand is expected to remain weak in the face of Congressional budget cuts. Since the majority of consumer electronics products (e.g., TV, stereo, VCR) sold in the United States are produced

off-shore with off-shore PWBs, changes in the domestic consumer market will probably have little effect on domestic PWB production. These trends are expected to continue for at least the near future.

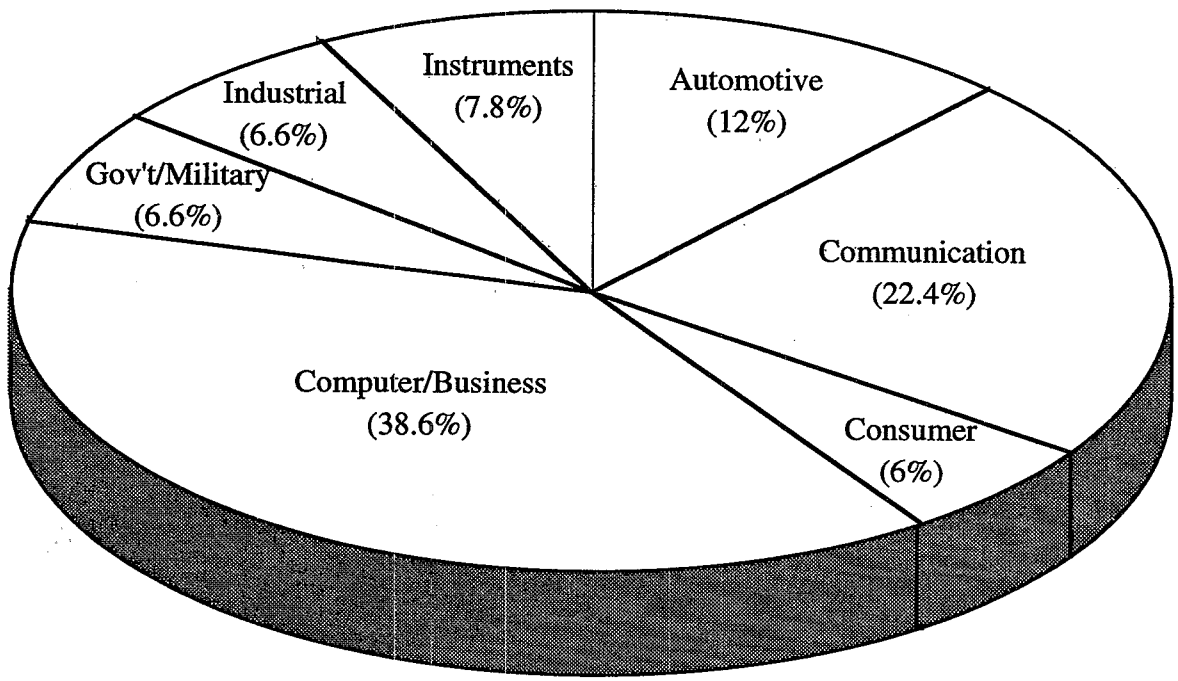

Figure 1-7. Market for PWBs in the United States in 1993.
Source: IPC Technology Marketing Research Council, June 1994.

E. Analysis of Laminates and Process Consumables for Rigid Boards

The printed wiring board product market is normally broken down in one of two ways: either by the type of substrate used (glass, paper, composite) or the type of board produced (single-sided, double-sided, multilayer). Table 1-4 shows the U.S. market summary for PWB production broken down by type of substrate used for rigid PWBs. Glass substrates compose the largest market segment by far. In addition to rigid PWBs, the United States also produces approximately $400 million of flexible circuitry.

As part of the 236 million square feet of laminate used in 1993, the PWB industry consumed approximately 587 million square feet of copper foil and 52 million pounds of epoxy resin. The industry also consumed approximately 60 million pounds of fiberglass yarns used in 322 million square feet of pre-preg. Pre-preg is un-cured epoxy-fiberglass material used to separate and electrically insulate the layers of circuitry in a multilayer PWB. Figure 1-8 summarizes the sales of various process consumables in 1993, such as drill bits, brushes, and tapes. These process consumables exclude laminates as well as other chemicals. The value of chemicals used in the industry was approximately $520 million. The primary chemicals used include the following:

- Plating chemistries (additive, electroless, electrolytic, etchback/desmear, oxide);
- Solder mask (dry film, photoimagible liquid, screen-defined);
- Etchants (ammoniacal, peroxide sulfuric, solder neutralizer);
- Imaging products (dry film, photoimagible liquid, screen defined, resist);

- Imaging chemicals (aqueous and insolvent developers and strippers); and
- Other chemicals (fluxes, metal strippers, cleaners, anti-tarnish, waste treatment chemistries).

Type of Substrate	PWB Dollar Volume	Laminate FT^2
Glass, 1-sided	$110.2	6.03
Glass, 2-sided	$1,115.0	64.08
Glass, thin	$2,892.3	118.0
High-performance	$458.0	7.0
Paper, 1-sided	$8.0	1.0
Paper, 2-sided	$0.0	0.0
Composite, 1-sided	$425.2	38.0
Composite, 2-sided	$48.8	2.0
Totals for Rigid PWBs	$5,057.6	236.0

Source: IPC Technology Marketing Research Council, June 1994

Table 1-4. Domestic Rigid PWB and Laminate Production by Type of Substrate Used (all dollars in millions/all square feet in millions).

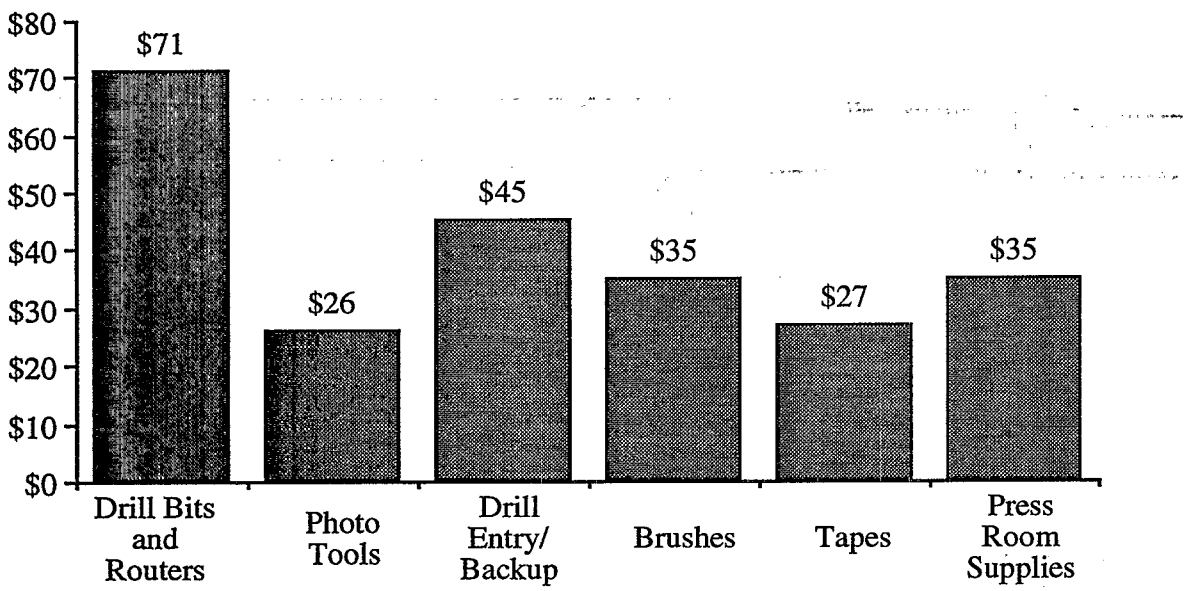

Figure 1-8. Sales of Various Process Consumables for Rigid Boards in 1993 (all dollars in millions). Source: IPC Technology Marketing Research Council, June 1994.

V. TECHNOLOGY TRENDS ANALYSIS OF INDUSTRY

PWB technology continually evolves—the major trends have focused on reducing the size and increasing the capacity of the PWB. These changes are often accomplished through advances in the following technologies: multilayer, surface mounting, fine-pitch, hole density, hole size, and multichip modules.

Using multilayer PWBs (especially high-layer count PWBs) increases capacity and reduces size by allowing more circuitry to be built into one PWB. Each layer has its own circuit pattern. Similarly, using surface-mount technology allows components to be placed on both sides of the PWB instead of just one side, as is the case with through-hole technology. With through-hole mounting, the pins or leads on the component are inserted through holes in the PWB and come out the other side, thereby using up space on that side of the PWB. With surface-mounted components, the pins or leads are attached to pads or lands on one surface of the PWB, so the opposite side of the PWB remains free for either other components or circuitry. A pad or land is the end of a circuit line or trace intended as the connection point for a component. Typically, the pad or land is significantly wider than the rest of the circuit trace in order to approximately match the width of the component lead that will be attached to it.

Pitch refers to the distance from a point on a particular feature to the same point on the adjacent feature. Pitch, as used by the PWB industry, frequently defines the distance from the center of a circuit line (also called "trace") to the center of the adjacent line. The thinner the line and space (or finer the pitch), the more lines can be placed on the PWB. Similarly, density refers to the percentage of the PWB covered by conductors or by components. To save routing space with large-pitch components, PWB designers run circuit lines in-between adjacent pads on which the component leads are mounted. High-density PWBs may have three or more conductors between the pads.

Another technique to reduce size and boost performance is to decrease the size of the vias or holes used to conduct electricity from one side of the PWB to the other or to an inner layer. Finally, another technology for increasing performance while decreasing size is multichip modules (MCMs). For most applications, the bare integrated circuit (IC) chip is sealed in a hermetic or plastic package before being mounted on the PWB. This package protects the IC from moisture and other hazards, but takes up space and increases weight. MCMs consist of multiple bare IC chips mounted directly on a substrate, often quite similar to a small PWB. This MCM can then be coated for protection and used as is as a special type of PWB or mounted on another PWB as part of a larger PWA.

A. Multilayer Technology

The following information on trends in multilayer technology, as shown in Figure 1-9, refers to the number of different layers used as a percent of all multilayer boards sold. Multilayer PWBs account for about 66% of the market, as discussed in Section IV.B. As evident from Figure 1-9, the relative distribution of three- to four-layer boards has been relatively steady for several years, while that of multilayer boards with nine or more layers has risen slightly over the past three years. In general, however, the production of two- to four-layer boards has declined over the past ten years from approximately 48% of the market in 1984 to 33% of the market in 1993. That decline has been matched by a rise in production of nine plus multilayer boards. The largest markets for multilayer PWBs are computers and communications where size and performance are critical. Consumer products use many single-sided PWBs because cost is paramount, while size and weight are less critical. For this same reason, the market uses many 1- and 2-sided PWBs.

B. Surface Mount

Surface-mount applications (as opposed to through-hole components) save space and allow increased component density on the printed wiring assembly. A history of the growth of surface-mount applications for independent PWB manufacturers is shown in Figure 1-10. In addition to rising surface-mount applications, the percentage of boards with surface-mount applications on both sides of

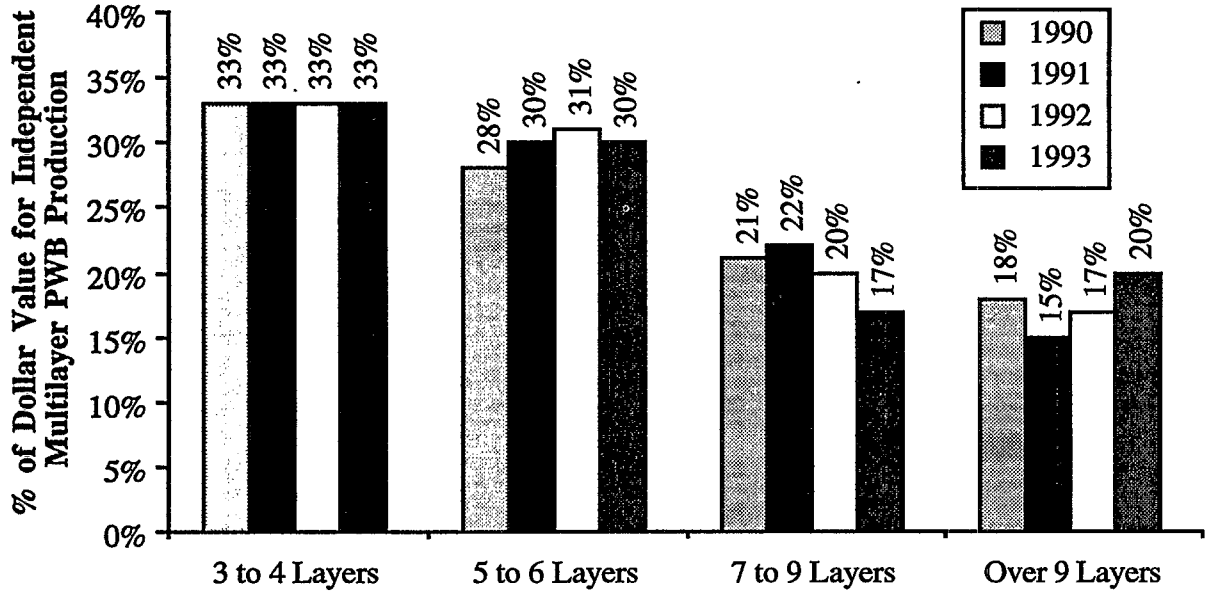

Figure 1-9. Historical Trends for Layer Count in Multilayer PWBs.
Source: IPC Technology Marketing Research Council, June 1994.

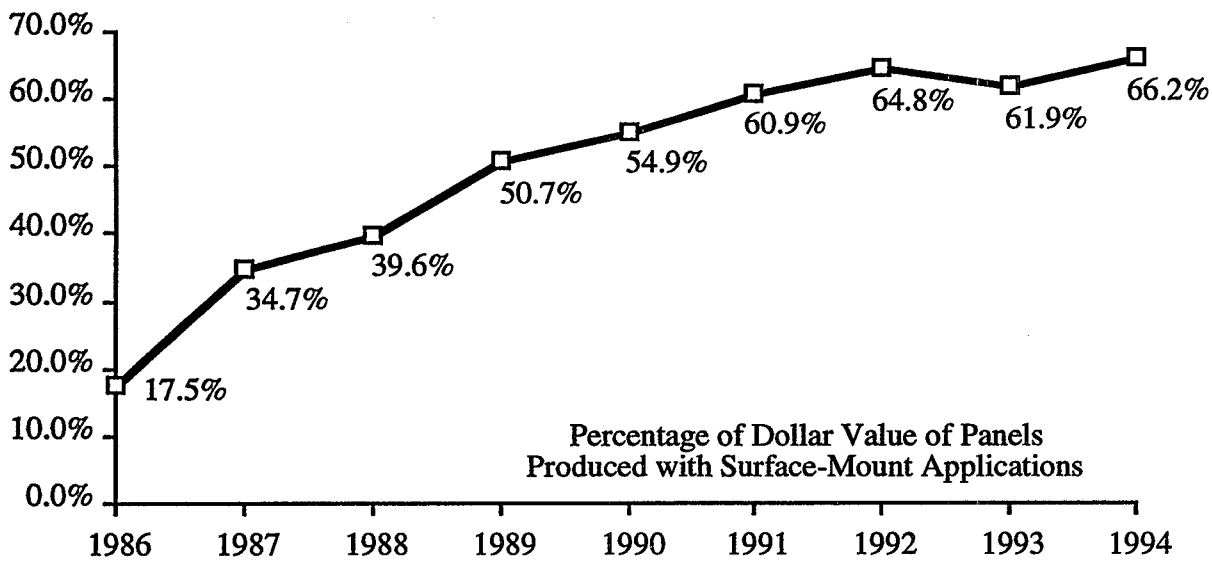

Figure 1-10. Historical Trends on Surface Mount Applications in PWB Production.
Source: IPC Technology Marketing Research Council, June 1994.

the boards has also been increasing steadily for at least the past seven years, which allows increased performance and decreased size. Of the percentage of all panels with surface-mount applications, the fraction with surface-mount applications on both sides of the panel has increased from about 6% in 1987 to around 21% in 1994. In addition, the percentage of PWBs with 100% surface-mount patterns (i.e., no through-hole components) has increased from about 4% of all panels in 1988 to around 10% of all panels in 1994.

C. Fine-Pitch

Fine-pitch technology is generally defined as boards with 15 to 25 mils (thousandths of an inch) applications. If the pitch is over 25 mils, the PWB is not a fine-pitch PWB. Ultra-fine-pitch applications generally refer to applications under 15 mils. The use of fine-pitch technology generally can be traced two ways: historically, and by type of PWB manufacturer (OEM vs. independent). With reference to the former, fine-pitch and ultra-fine-pitch applications have been increasing steadily since the industry began collecting data in 1989. Now, approximately 20% of all PWBs produced have fine-pitch applications, and 45% of surface-mount PWBs have fine-pitch applications. This is approximately double the percentages of five years ago. In addition, ultra-fine-pitch technology is used in about 2% all boards and 4% of surface-mount boards (Figure 1-11). Two factors drive increasing fine- and ultra-fine-pitch technology: the demand for higher performance with reduced size, and increasing technological capabilities that allow fine-pitch PWBs to be produced more reliably.

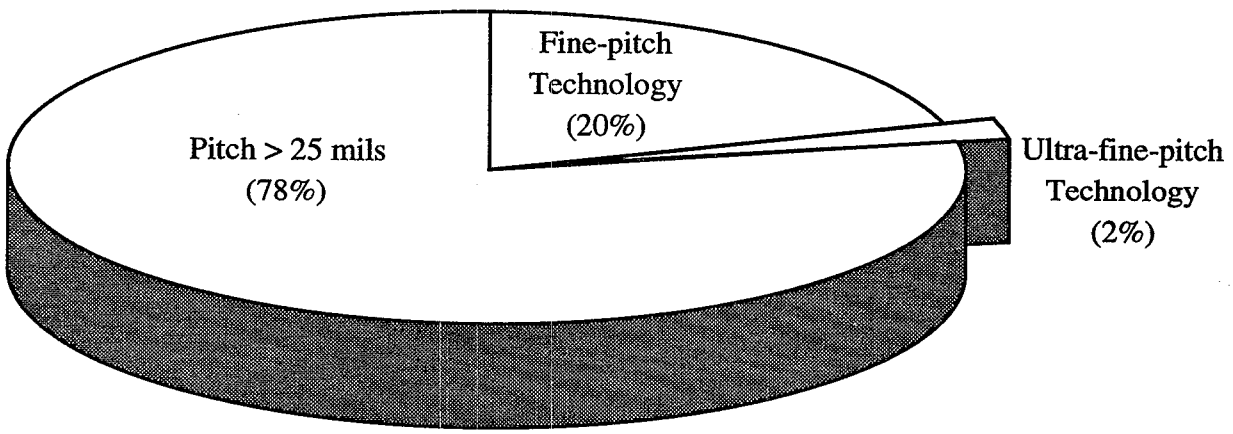

Figure 1-11. Use of Fine-pitch Technology.

D. Density and Hole Sizes

For this report, the criteria used to measure density applications is the volume of PWB production with a certain number of conductors between lands on 100-mil (0.100") centers (center refers to the center of the land). Density, in this instance, refers to the number of conductors between lands. Thus, a board with no conductors between 100-mil lands is very low density. The data on density production in 1993 is shown in Figure 1-12.

The majority of PWBs produced are medium to high density, with two or three conductors, respectively, between lands. As is often the case, demand for higher performance and smaller size drive higher densities, while cost constraints drive lower densities. High-density PWBs are usually more ex-

pensive to produce because of the yields and the greater level of testing that is required (e.g., optical testing of inner layers prior to lamination). The historical trend for density can be summarized as follows: low-density applications (0 to 1 conductors between 100 mil centers) have been steadily declining for approximately 10 years, medium-density boards (2 conductors between 100 mil centers) have remained steady at around 26% to 32%, and high-density applications (3 or more conductors between 100 mil centers) have been steadily increasing over the same time. Thus, the performance/size demands are slowly winning over the cost constraints. At the same time, the technology for producing high-density PWBs has been improving.

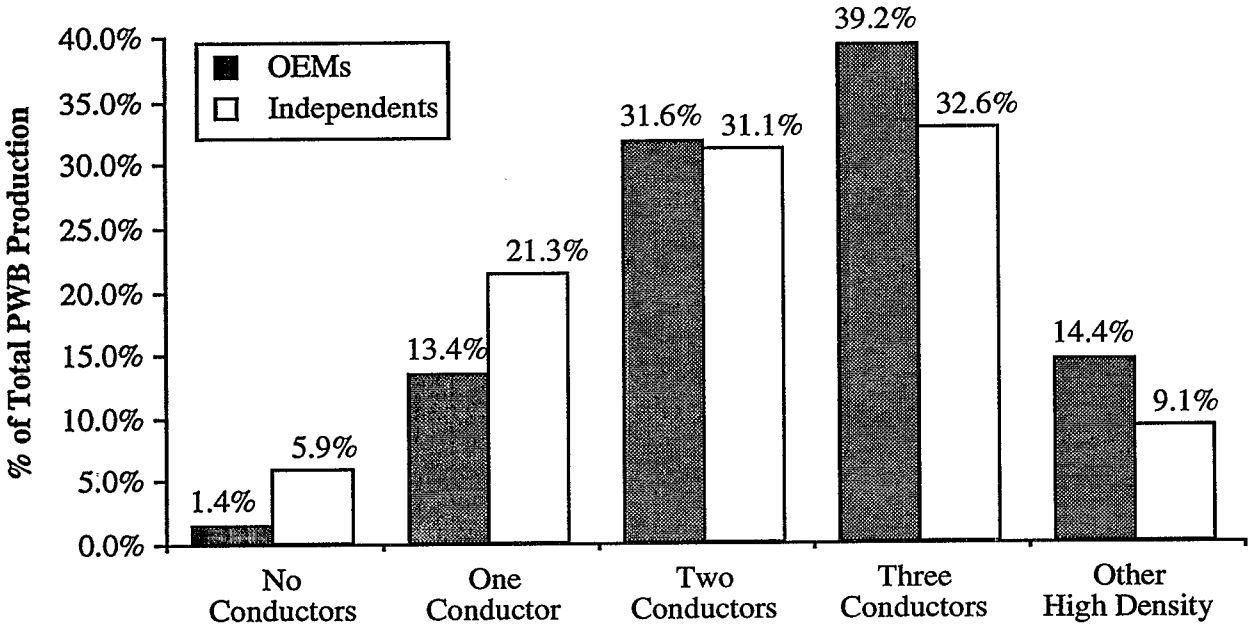

Figure 1-12. Density of PWB Production Based on Dollar Value of Production: OEM vs. Independents. Source: IPC Technology Marketing Research Council, June 1994.

With respect to hole sizes, an overview of percent of production for various hole sizes in 1993 based on dollar value of production is shown in Figure 1-13. In general, use of smaller holes (0.019" or less) has been steadily increasing over the past 10 years from approximately 7% in 1985 to over 40% in 1993 (Figure 1-14). Once again, smaller holes are generally more difficult and expensive to produce, but they do save space.

E. Plating and Coating

Platings and coatings on PWBs are primarily used during fabrication for the following purposes: as an etch-resist (typically tin-lead plating); to ensure solderability, typically tin-lead plating or flowed-on solder through HASL (Hot Air Solder Leveling); to protect against moisture or oxidation (often a conformal coating or solder mask); or to mask (cover) certain parts of the PWB against being plated with solder (solder mask). Following are two historical charts on the various types of surface finish and plating or coating techniques used by the PWB industry for the past four years (Figures 1-15 and 1-16).

The use of liquid film solder mask and photoimagible dry film solder mask has been generally declining, while the use of photoimagible liquid solder mask has been generally increasing. In addition, for the past four years, the industry has been trying to reduce lead consumption by eliminating tin-lead plating on boards, substituting instead tin plating or organic coatings.

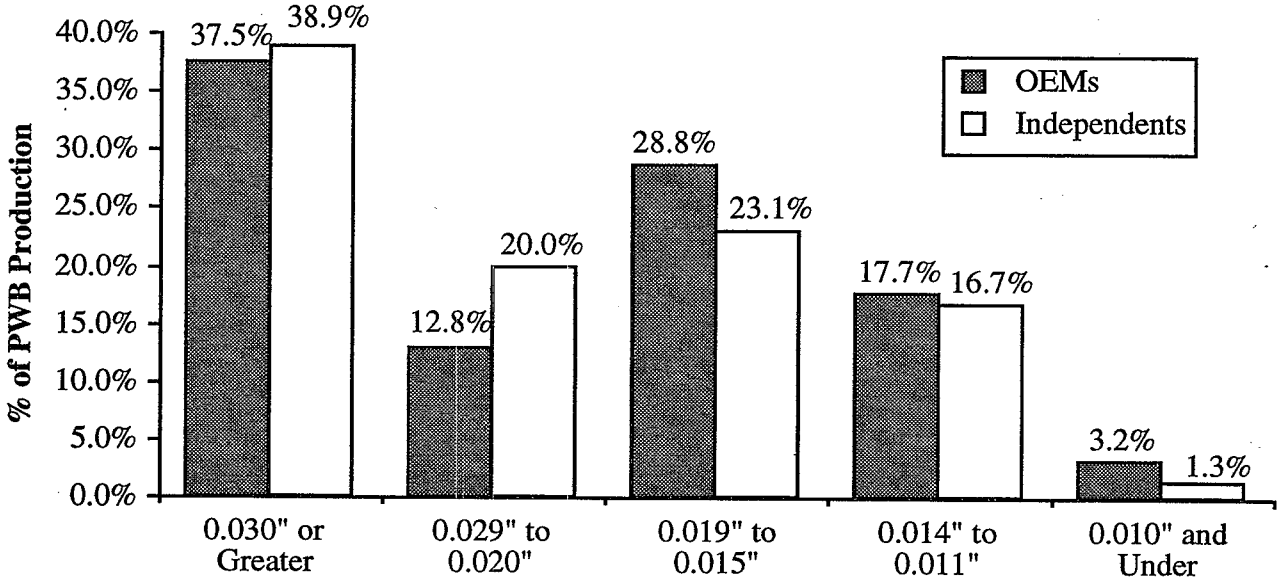

Figure 1-13. Percent of Production for Various Hole Sizes Based on Dollar Value of Production for 1993. Source: IPC Technology Marketing Research Council, June 1994.

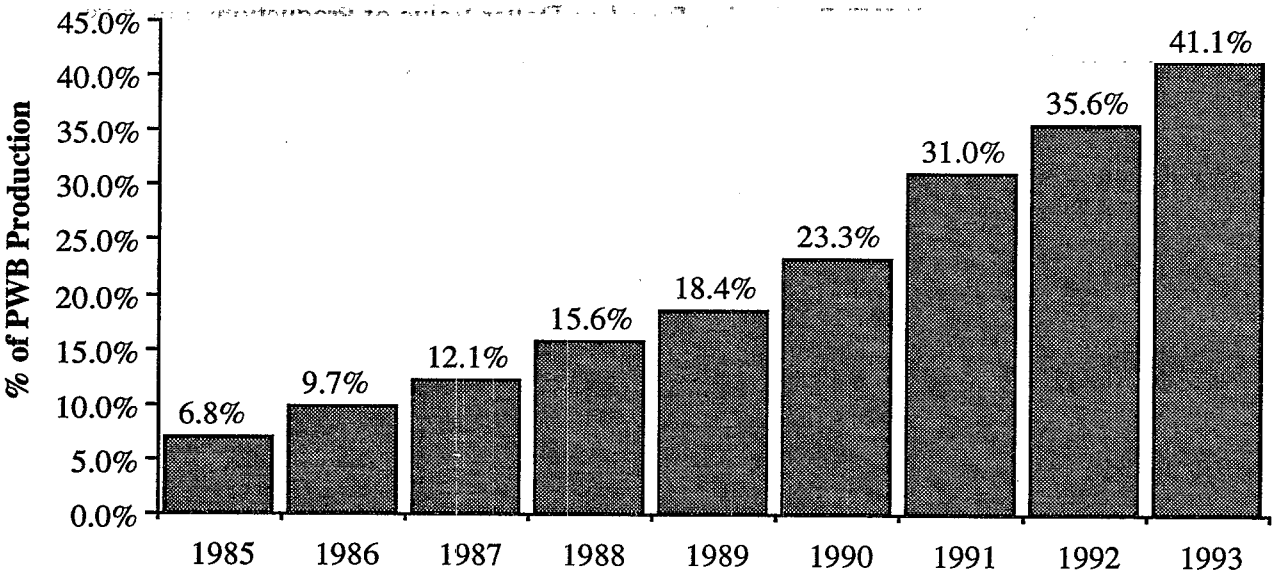

Figure 1-14. Percent Usage of ≤ 0.019" Holes from 1985 through 1993 Based on Dollar Value of Production. Source: IPC Technology Marketing Research Council Technology Trends Report, 1993.

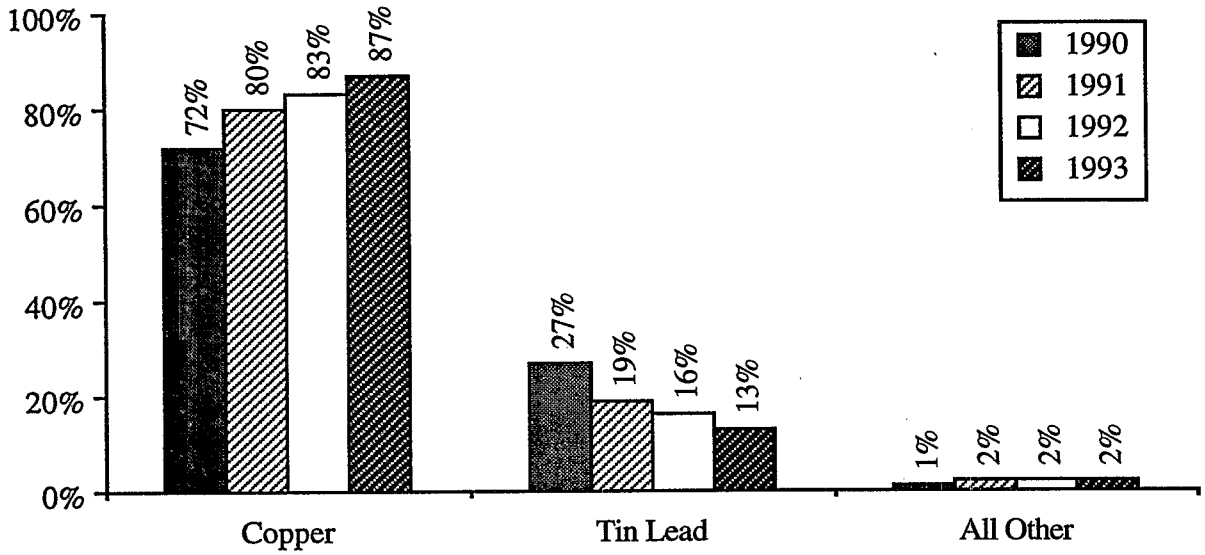

Figure 1-15. Historical Trends in PWB Surface Finish Techniques Based on Dollar Value of Production. Source: IPC, Technology Marketing Research Council, June 1994.

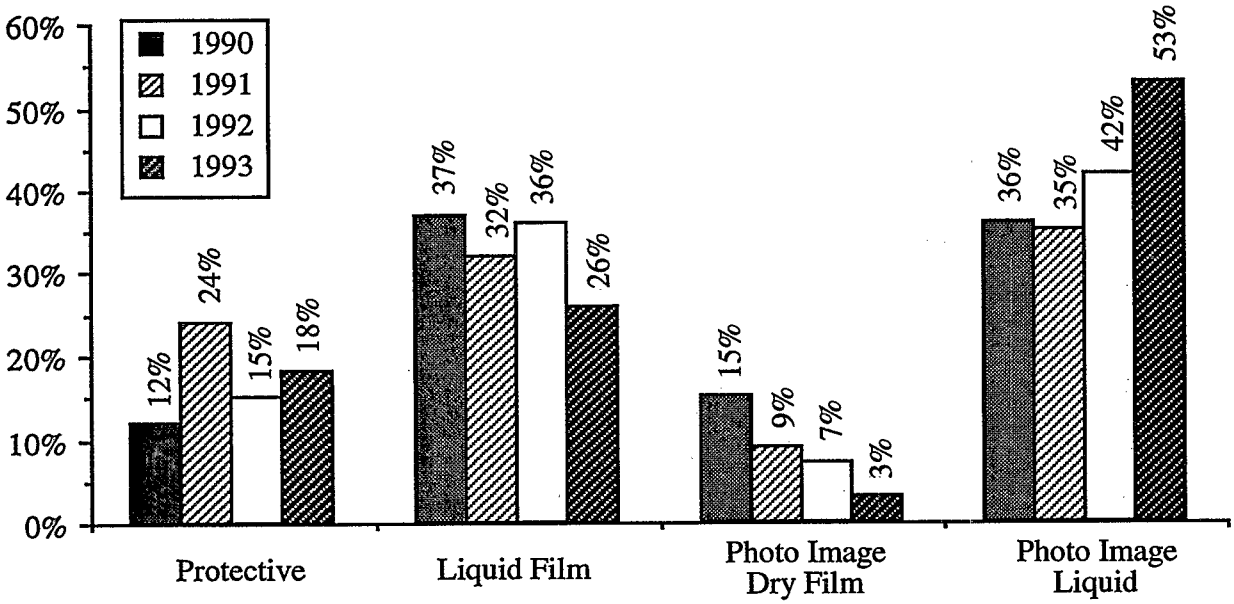

Figure 1-16. Historical Trends in PWB Protective Coating Techniques. Source: IPC Technology Marketing Research Council, June 1994.

F. Multichip Modules

The traditional and still most widely used methods for packaging ICs or "chips" are either surface-mount packages or plated through-hole (PTH) packages. However, in recent years new packaging/assembly methods have been developed, including bare chip attachment methods such as chip-

on-board (COB) and MCMs. Although MCMs are still not widely used, this packaging/assembly method is expected to increase in the near future as shown in Figure 1-17.

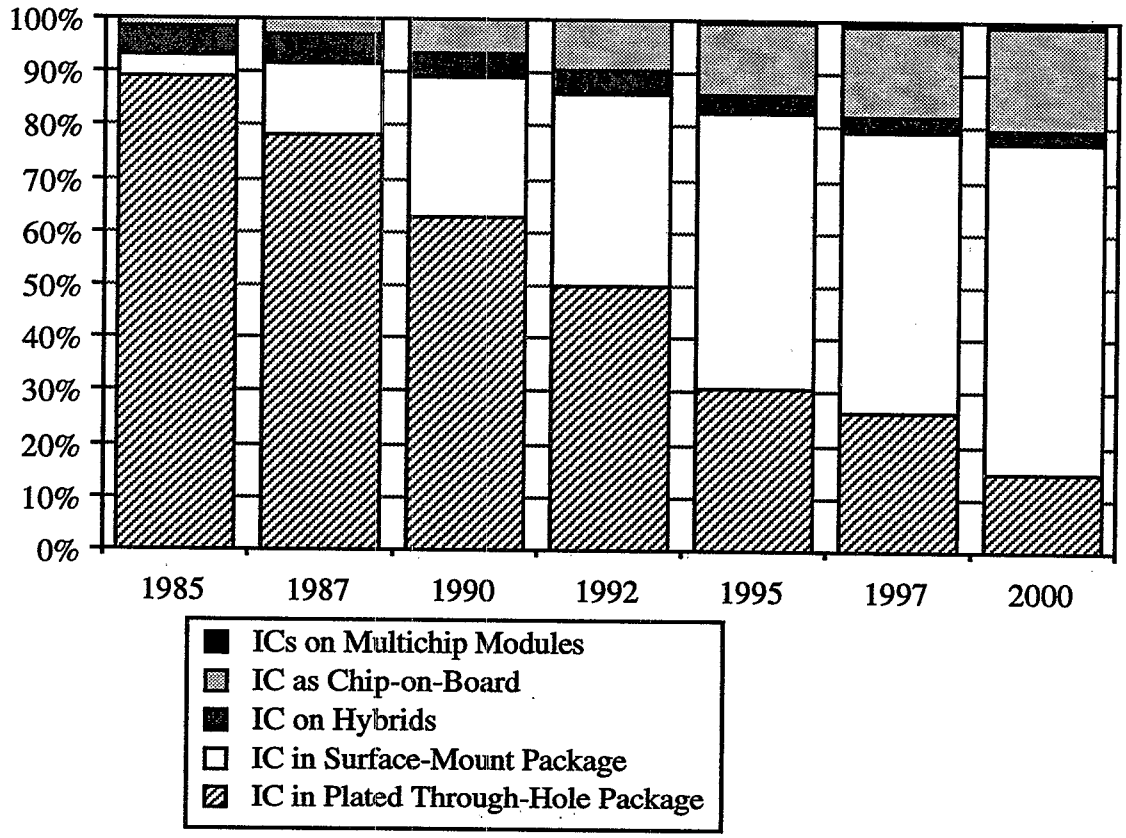

Figure 1-17. Worldwide IC Packaging Methods.

The advantages of multichip modules include the following:

- Interconnect a variety of bare, high-pin-count chips;
- Substantially reduce substrate area and signal delays;
- Reduce second level interconnection density;
- Improve electrical performance and heat extraction;
- Reduce system costs and design time;
- Mix digital, analog, and optical chips; and
- Incorporate discreet components in the substrate.

The three basic MCM types are defined by the type of substrate used and are as follows:

- Ceramic multichip modules (MCM-C), which use ceramic materials as a substrate;
- Deposited dielectric multichip modules (MCM-D), which use deposited dielectric films and metal conductors, similar to integrated circuit technology; and
- Laminate multichip modules (MCM-L), which use existing PWB materials, technologies, and facilities. MCM-L assemblies are smaller PWBs with a high packaging density and fine lines and spaces of interconnect.

PART TWO:

PRINTED WIRING BOARD USE CLUSTER PROFILE

I. OVERVIEW

A. Introduction

Printed wiring boards (PWBs) form the basis for interconnecting the devices and components in the vast majority of electronic products. Without this critical component, most electronics products could not function or would be significantly more expensive if constructed with other interconnect technologies. This use-cluster profile will describe the PWB fabrication process for the largest product segment of the industry, the rigid multilayer PWB. The profile focuses on the "subtractive" process, as it is the only broadly implemented approach to fabricating PWBs. Fully "additive" approaches are under development, which would radically change the overall process flow and are described briefly in the Sections I.C.5 and I.C.6.

B. Use Cluster Profile

A use cluster is a set of chemicals, processes, and technologies that can substitute for one another to perform a specific function. A use cluster profile of the PWB industry, therefore, describes alternate chemicals, processes, and technologies that may be used to complete each step or function in the entire PWB manufacturing process.

This use cluster profile is intended to aid in the selection of a use cluster for assessment in a Design for the Environment (DfE) project. The profile identifies different processes in the PWB industry (e.g., laminating, making holes conductive) and steps within those processes (e.g., imaging, etching, plating). The process steps are described in flow chart form with a description of each step. Next, the chemicals, materials, and technologies used in each step are briefly described. The profile may also mention commonly accepted alternatives to these practices, and processes or materials that are recognized to have especially high environmental impacts. Information on the risk and releases of these materials can then be used to target areas for further work.

C. Overview of PWB Types and Manufacturing Methods

Printed wiring boards are categorized in several ways. When overall complexity is being considered, they are often categorized in terms of layer-counts, or the number of circuit layers present on a single PWB. PWBs are usually broken down along layer-count lines into three categories: multilayer, double-sided, and single-sided. Multilayer PWBs contain more than two layers of circuitry, i.e., at least one layer is imbedded in the substrate beneath the surface of the board. A multilayer board may consist of 20 or more interconnected layers, but more common are 4, 6, and 8 layers. Double-sided boards have two interconnected layers and are generally easier to produce than multilayer PWBs, while single-sided PWBs have only one layer of circuitry.

PWBs are also categorized by substrate, or base material, type and fall into three basic categories. Rigid PWBs typically are constructed with glass-reinforced epoxy-resin systems that produce a rigid board at thicknesses of less than 0.1" (0.062" is the most common rigid PWB thickness, although there is a trend toward thinner PWBs). Flexible (or flex) circuits are manufactured on polyimide and polyester substrates that remain flexible at finished thicknesses—ribbon cables are common flexible circuits. A third category of PWBs consist of boards that are essentially combinations or assemblies of the first two: rigid-flex combinations of one or more rigid PWBs that have one or more flexible circuits laminated to them during the manufacturing process. Three-dimensional circuit assemblies can be created with rigid-flex combinations.

Manufacturing methods can be boiled down to two types, although hybrid methods exist. Most common is subtractive processing, in which copper is selectively removed from a PWB to form a circuit. Within this process, however, copper and other metals are also added during plating steps. The term "subtractive" refers to the method of image transfer from a photo-tool or image file to a copper circuit on a PWB. Additive processing refers to a process in which an image is formed by selectively adding copper (electrolessly plating onto a substrate an image of a circuit). In a fully additive process no etching, or removal of copper, occurs.

As part of an industry driven activity, the 1994 Electronics Industry Environmental Roadmap[2] described a generic PWB process, developed in conjunction with the IPC, with comments from technical experts participating in the process (Figure 2-1). Representative of the highest value segment of the PWB market, this process flow is indicative of the manufacture of rigid multilayers. This process description was used as a baseline for selection and definition of the use clusters in this analysis.

1. Single-sided Manufacturing Overview

Single-sided PWBs continue to be manufactured in high quantities in term of units (71% of PWBs manufactured in the U.S.), but represent only 10% of the total value of U.S. production. Single-sided PWBs are comparatively easy to produce and the market is highly competitive, as demonstrated by the fact that a single-sided PWB costs only about one-tenth that of a double-sided PWB.

Several critical manufacturing steps are not included in the typical single-sided manufacturing sequence and no process is unique to single-sided production. Therefore, any manufacturer of double-sided or multilayer PWBs can produce single-sided ones as well. Few shops produce single-sided panels exclusively, but instead include single-sided PWBs as part of their overall product mix. Many shops do not produce single-sided panels at all due to the market conditions mentioned above.

The most common sequence of single-sided production is drill, print-and-etch, surface finish, and final fabrication. No inner-layer processing is required, and desmear is also eliminated. Furthermore, only in rare cases are plated through-holes required, therefore, the entire cluster of making holes conductive is not applicable to single-sided manufacturers. The holes instead provide mechanical stability for through-hole panels. Drilling may be completely eliminated on single-sided PWBs if the components are all surface-mounted. Alternative methods of single-sided manufacturing are available. For example, for prototyping, single-sided PWBs can be created by selectively milling or routing copper with an NC machine, thereby forming a circuit without using wet processes at all. Other table-top prototype systems have also been devised.

2. Double-sided Manufacturing Overview

Not unlike single-sided, double-sided PWB manufacturing is also a subset of the multilayer process described in Section II. The inner layer image transfer, lamination, and hole cleaning clusters are not performed. Therefore, any multilayer manufacturer can easily produce double-sided panels and most do so. Double-sided PWBs do require electroless copper or other methods of making holes conductive, since the top and bottom sides of the board require interconnection.

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2 Pedersen, Pitts, et al., Electronics Industry Environmental Roadmap, MCC, 1994, p. 39.

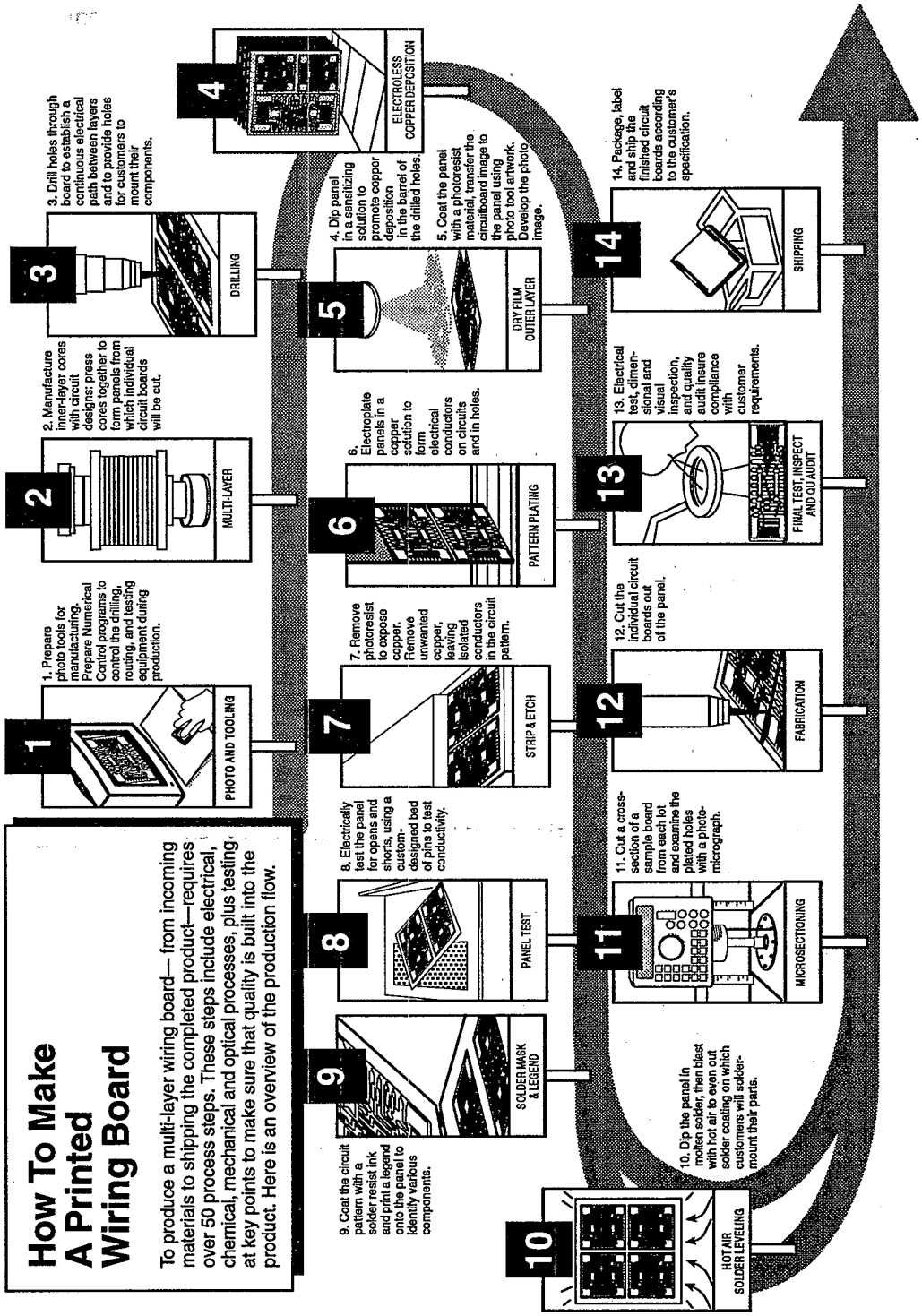

Figure 2-1. The Basic Manufacturing Flow for the Fabrication of Rigid Multilayer PWBs.[3]

3 Pedersen, Pitts, et al., Electronics Industry Environmental Roadmap, MCC, 1994, p. 39.

3. Multilayer Manufacturing Overview

Single- and double-sided manufacturing processes are subsets of the multilayer process. Thus, it is logical to use the multilayer process as the focus of this profile. In addition, multilayer boards represent two-thirds of the overall value of U.S. production dollars, even though they are produced in lower numbers than single- or double-sided PWBs. The rigid multilayer process (rigid PWBs represent about 95% of U.S. production) is discussed in detail in Section II.

4. Flexible PWB Manufacturing Overview

A flexible circuit is manufactured on materials that allow for the bending or flexing of the PWB to create a three-dimensional effect. Flex circuits may be designed to be bent into shape once or a few times, or to withstand thousands of flexing cycles. They are found in printers, disk drives, automobile electronics, and a wide range of other common products.

Although similar to rigid manufacturing in many respects, the flexible circuit manufacturing process deals with unique materials and surface finishes, and the process is not integrated into a rigid PWB shop without considerable effort. Therefore, few rigid manufacturers have expanded into the flex market. On the other hand, because an important portion of the flex market is rigid-flex combinations or assemblies, manufacturers of predominantly flex substrates often produce rigid boards as well. Because flexible substrates have larger dimensional tolerances than rigid ones, multilayer flexible circuits are more difficult to manufacture and are less common than rigid multilayer PWBs.

Image transfer, drilling, and through-hole plating are performed in a similar, but not identical manner. Flex substrates are thin and are unlike standard rigid materials—some common flex materials are polyimide and polyester, although many others are in use. Thicknesses of only a few mils are common compared with inner-layer rigid material thicknesses of up to 31 mils, and double-sided thicknesses of 62 or more mils. Additionally, tooling and surface finish processes for flexible circuits are quite different from those of rigid PWBs. A cover sheet of similar material to the base film is applied over typical flex circuitry rather than a solder mask and is press laminated over the circuitry. The cover sheet is pre-punched to expose appropriate areas of the circuit for soldering of components and connectors. Not all flex circuits require solder; those that do are hot-air or hot-oil solder-coated. Nickel-gold is also a common finish.

5. Subtractive Overview

The fabrication of PWBs through the years has relied mainly on a subtractive print and etch process for forming copper conductors. The process flow shown in Figure 2-1 describes such a subtractive approach. In a subtractive process for rigid multilayer PWBs, metal is removed from a solid foil to form the desired interconnect pattern for the inner layers, as shown in Figure 2-2 and described below. The label subtractive comes from the typical processes used for making these inner layers, encompassed in step 2 of the overall process shown in Figure 2-1.

As shown in Figure 2-2, the subtractive process begins with copper-clad laminate, composed of a thin copper foil covering both sides of the epoxy-glass core material (a). The laminate is coated with a sacrificial photopolymer material that acts as a resist in subsequent steps (b). The resist is photoimaged (exposed/developed) to expose the copper to be removed (c). The board is then etched, after which the resist material is stripped and disposed in a fabrication waste stream, leaving the desired interconnect pattern in copper on the exposed laminate (d). In a multilayer structure, each of the inner layers is constructed independently, then laminated together using a B-stage epoxy in between each inner layer core

to form the overall structure (e). This non-sequential process of building multilayers is essentially independent of the number of inner layers laminated together and is used to build PWB structures with any number of layers.

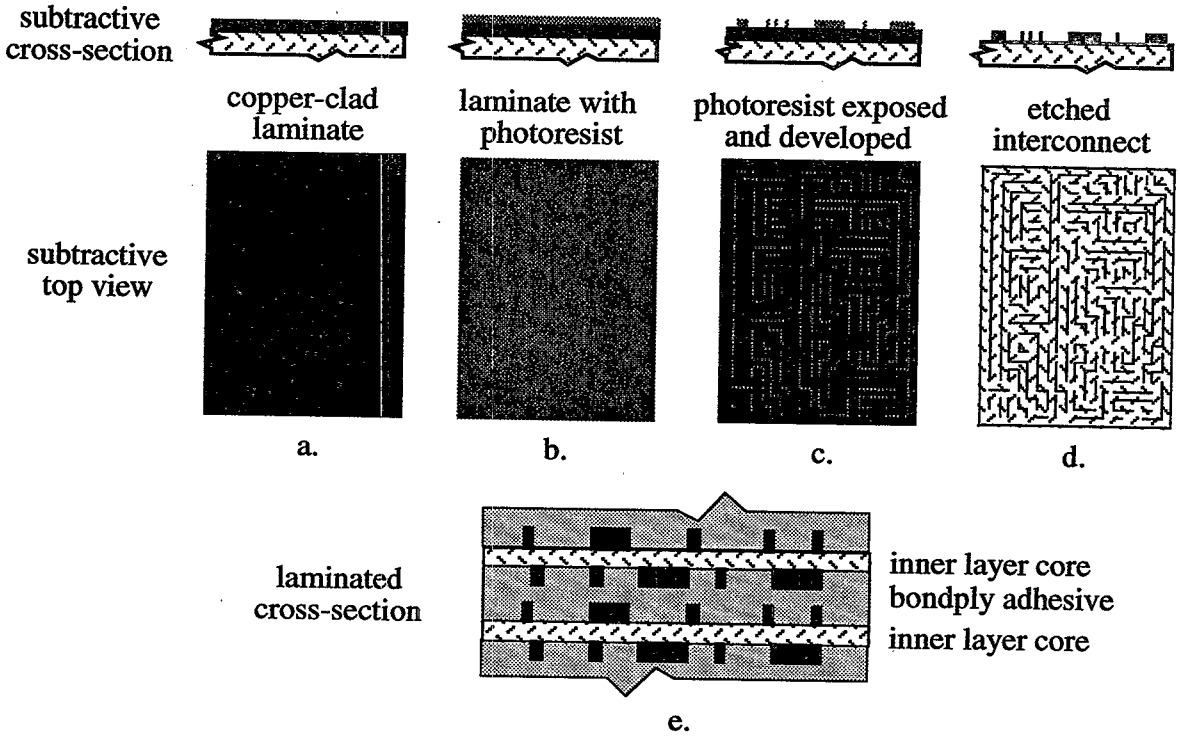

Figure 2-2. The Simplified Subtractive Process for Manufacturing Inner Layers of Rigid Multilayers (a through d), and a Cross-Section of Two Inner-Layer Cores within a Multilayer Structure (e).

6. Additive Overview

Full-build additive approaches for double-and single-sided boards have been in use for over 20 years. Processes that use full build to make multilayer boards have only recently been under development in this country, and none are in widespread use. Since the additive deposition of seed layers is used for electroplating at certain steps within a subtractive process flow, the full-build descriptor is intended to describe a process where the metal deposition is fully additive, eliminating all etching steps. The intent of these novel approaches is to take advantage of the PWB industry's current capabilities in photoimaging and printing as used in subtractive processes, while overcoming the limitations and expense of plating, etching, and lamination, as well as eliminating the drilling of vias to form the vertical interconnect between layers.

Each layer is built upon the previous one, so this type of additive approach is also known as a sequential build. As such, there is no lamination step required. Yield considerations become more critical in sequential processing, because an irreparable flaw in the final layer destroys the entire structure. In subtractive processing, the inner layers can be inspected prior to lamination to ensure a higher overall yield.

As shown in Figure 2-3, the additive process for rigid boards begins with a bare catalyzed laminate with no metal on the surfaces (a). Alternatively, with some processes, the first layers on either side of the core laminate are etched to form power and ground planes and may already have plated through-holes. The laminate is coated with a permanent photodielectric material that acts as the dielectric separating the metal layers (b), thus replacing the subsequent core and B-stage layers in the subtractive approach. The dielectric is imaged and developed to form the vias, then a second layer is applied to form the interconnect pattern (c). The board is then selectively plated or metallized by other means, forming the desired interconnect pattern (d). In a multilayer structure, steps (b), (c), and (d) are repeated to form the overall structure (e). In contrast to the conventional subtractive process described previously, this process requires no lamination, with the unreinforced layers built sequentially on the initial rigid core.

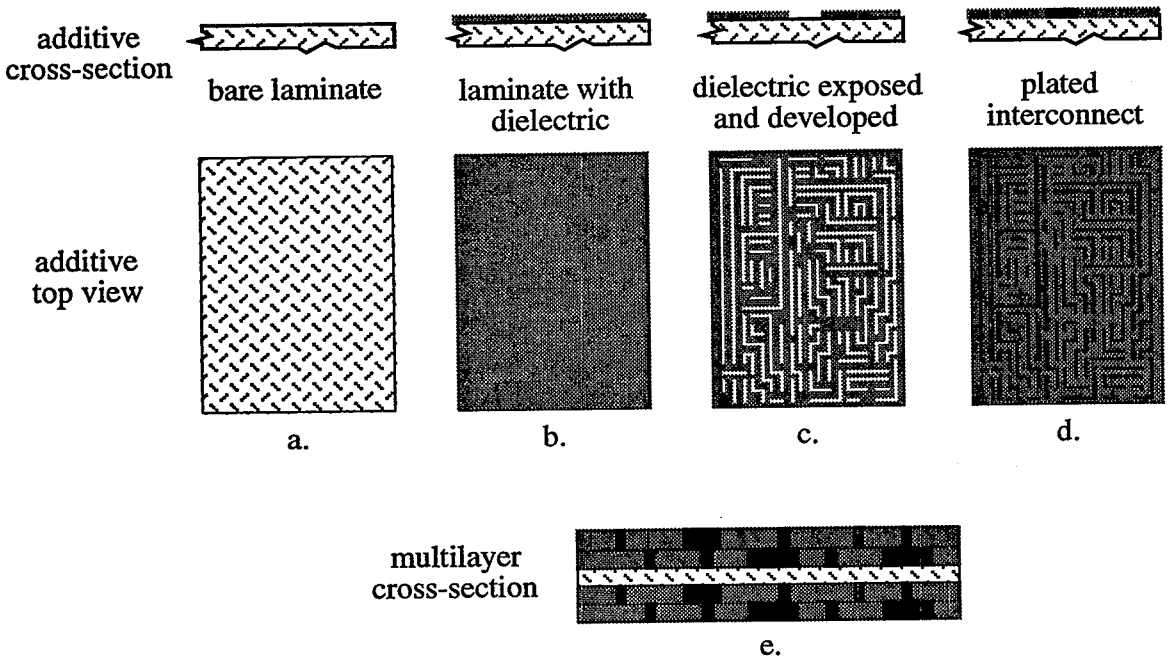

Figure 2-3. The Simplified Full-Build Additive Process for Manufacturing Inner Layers of Rigid Multilayers (a through d), and a Cross-Section of a Multilayer Structure (e).

7. Additive Metallization Techniques

Several methods are under consideration for deposition of the circuit traces and vias in an additive structure. None of these methods have been broadly commercialized due to either the maturity, the economics, or outstanding technical challenges. Current research is addressing all of these issues.

a. Solid Systems

The most conventional approach to additive electroless copper plating is to catalyze the entire surface of a bare laminate board by preparing it with liquid solutions containing a latent oxidizer such as ionic tin. Colloidal palladium is applied to the surface and oxidized to the catalytic pal-

ladium form. The catalyzed surface is masked using either a temporary or permanent resist. The remaining exposed surface is then plated electrolessly, with the copper adhering only to the exposed catalyzed areas. In some cases photosensitive materials are used to coat a dielectric and then dried to form a catalytic coating. The coating is made selectively catalytic to electroless plating by exposure to light.

The disadvantage of these approaches is that the latent catalyst is left buried under subsequent layers or under any type of permanent resist or dielectric that is used to planarize the circuits. The latent catalyst is a potential source of ionic contamination and possible metal migration and dendritic growth.

In another additive approach, a permanent dry film material is used to build double-sided boards using laminate material with a special catalyst layer. The dry film is laminated, exposed, and developed in the conventional manner and then cured on the board. The exposed catalytic layer is conditioned to expose the catalytic material in it and to provide a better surface for metal adhesion. This is followed by the electroless bath. A process patented and demonstrated by DuPont uses the adhesive characteristics of photopolymers to selectively adhere to metal particles in unexposed areas. The metal particles then catalyze the surface for electroless plating.

b. Screen Printing

One method for image transfer in the fully additive process is screen printing. Screen printing is limited to applications where trace lines are large (>0.008"). In this method, permanent plating resist is printed onto a laminate that either has been or can be made catalytic to electroless plating. The plating resist is screen printed in the reverse image of the circuit lines and copper is plated on the exposed catalyzed laminate. The plating resist is not later etched, but remains as a permanent dielectric. In addition to the fact that this method uses fewer steps and generates less waste, it has the additional advantages of:

- Leaving a planar surface after metallization, and
- Leaving a surface where solder is attracted to conductors and repelled from the smooth dielectric material. The second point allows for some degree of self-alignment during surface mount.

The disadvantages of using a screen-printed liquid resist are the following:

- Multiple passes may be required to build up sufficient thickness to match the thickness of the lines to be plated, and
- Most screen-printable resists contain significant amounts of volatile organic compounds which must be captured and either recycled or incinerated (oxidized).

Other methods of image transfer used for additive processing include screen printing of conductive polymers and screen printing sinterable metal particles suspended in a polymer matrix. In both of these cases, trace line resistivity is more than one order of magnitude above that of pure copper.

c. Liquid

Liquid materials can be used to transfer the actual circuit lines themselves. In these processes, a plating catalyst is bound to a photosensitive material. There are examples of both positive and negative working photosensitive materials systems, although none have been put into volume production. For example, D'Amico and DeAngelo have developed a process called photosensitive

metal decomposition (PSMD).[4] In this case, stannous oxide (SnO) takes one of two reaction paths, depending on whether or not it is exposed to UV light. If exposed, SnO is oxidized to form stannic oxide (SnO_2). SnO_2 cannot reduce Pd^{+2} to its metallic form. However, if UV light is not present, then SnO_2 in a caustic environment reduces palladium chloride (Pd^{+2}) to palladium (Pd°). Pd° is a catalyst for electroless copper deposition. Since light is used to prevent catalyst formation and signal line deposition, this process is negative working. As such, it is prone to unwanted copper deposition and shorting due to factors such as particles on the laminate surface or photo-tooling.

Iwaki has developed a process called "photochemical circuits."[5] In this process, a silver salt is decomposed using ultraviolet light, leaving small sights of reduced silver metal.

$$R{\bullet}Ag + h\mu \rightarrow Ag + R$$

This process is positive working since light is used to form the catalyst for electroless metal deposition where exposed. Positive working processes tend to have a higher yield than negative ones. This has been demonstrated in the fabrication of integrated circuits. However, silver is highly mobile and can cause other yield problems because of its mobility. It is also expensive and can form highly unstable salts.

Frisch developed a positive working process called photo formation (PF).[6] Here, copper metal salt in the form of cupric acetate (CuXX) can be reduced to Cu° by exposure to UV light. The reaction requires a UV-sensitive reducing agent to be present. The reducing agent, diazoquinone, is also used in photoresists for integrated circuit processing.

Mansfeld and Jans developed a process called physical development-reduction (PDR).[7] In this process, titanium dioxide (TiO_2) particles disbursed into the adhesive are the light-activated reducing agent. A thin layer of Pd^{+2} is coated over the adhesive. When exposed to UV light, TiO_2 is further oxidized and releases electrons that reduce Pd^{+2} ions to metal form.

$$TiO_2 + h\mu \rightarrow TiO_x + 2e^-$$

$$2e^- + PdCl_2 \rightarrow Pd^{\circ} + 2Cl^-$$

Printron, Inc., developed a process called the Printron Process.[8] In this approach, image transfer can be done via either screen printing (low-density, low-cost) or electrophoretic deposition (high-density and higher costs). This is a positive process where fine solid metal particles are suspended in a proprietary "ink." After the image is transferred in a mode compatible with the cost and density goals, the metal particles are melted using electromagnetic fields. In this way, only the metal is heated. Though promising, this method has not become a dominant product in the market.

d. Sequential Build

One concept under development utilizes a photoimagible dielectric to produce the pattern for vias and interconnect traces. This approach eliminates the need for a separate dielectric and

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4 J. F. D'Amico and M.A. DeAngelo, *J. Electrochemical Soc.*, Vol. 120, No. 11, 1973, p. 1469.
5 A. Iwaki et al., *Photographic Science Engineering*, Vol. 20, No. 6, 1976, p. 246.
6 D.F. Frisch, *Electronic Packaging and Production*, February 1985, pp. 194-203.
7 J.F. Mansfeld and J.M. Jans, *Plating and Surface Finishing*, Vol. 66, No. 1, 1979, p. 14.
8 K. Krubsack, Guide to the PWB Marketplace, Ed. by C. Lane & G. Mancuso, 1993, Chapter 37, pp. 37.1-37.3.

clad metal layer that requires either etching or a combination of plating and etching to produce a circuit. It also eliminates the resist deposition and stripping previously required to define that circuit.

No additional drilling is required to form the vertical interconnect between layers. The connection between layers is formed during the sequential steps described. Any vias desired through the starting core material are formed by conventional drilling and plating techniques prior to the sequential build of interconnect layers.

II. CLUSTERS FOR RIGID MULTILAYER PWB MANUFACTURING

For purposes of this use cluster profile, the fabrication of rigid multilayer PWBs has been broken down into nine process steps (see Figure 2-4). These steps form a generic process flow, with many processes and potential alternative processes within each function. Each process step and its associated use cluster is described below, identifying the most common processes, alternatives (where appropriate), and the general technology trends.

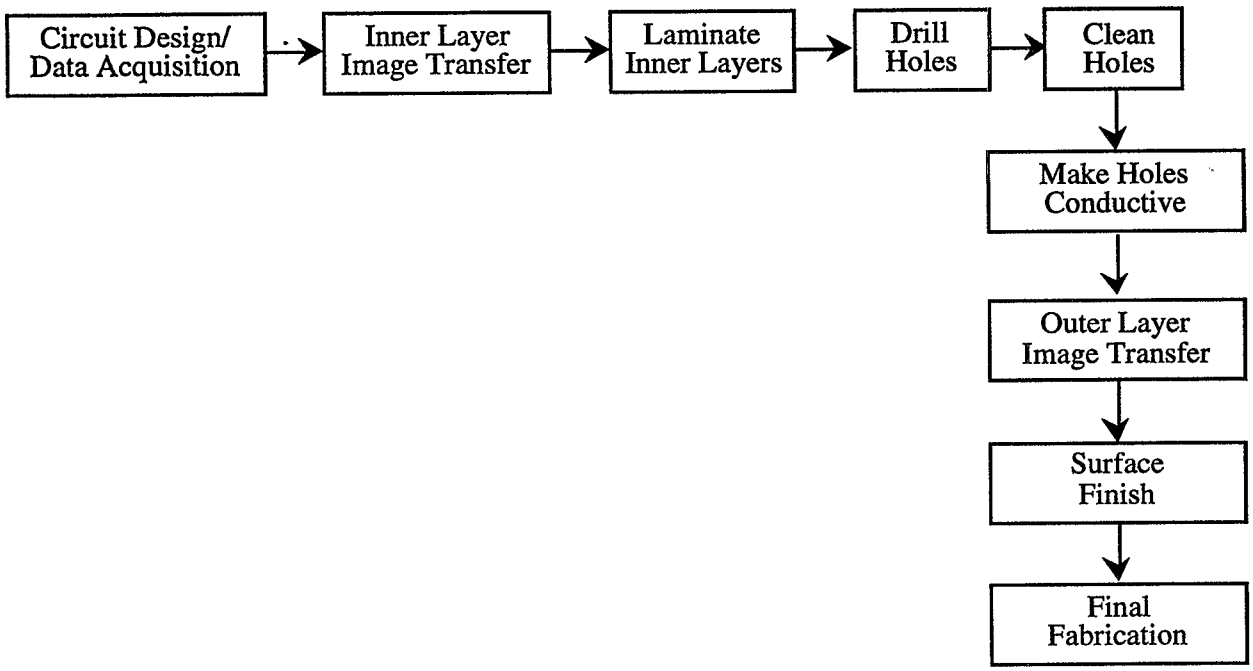

Figure 2-4. Typical Process Flow for PWB Manufacture.

A. Data Acquisition and Computer-aided Design (CAD)

The method by which PWB shops receive circuit images and other data has changed dramatically over the past 15 years. As late as 1980, manual methods of circuit layout were not uncommon. These included the familiar hand-tape method, whereby a layout artist would apply strips or doughnuts of black tape onto a mylar sheet. The resulting circuit artwork, usually on a 2: or 4:1 scale, would be submitted either to a photographic service bureau or the PWB shop for photographic reduction. Photo-tools were created from contact prints of the reduction. Paper plots from early computer-aided design (CAD) systems were also photographically reduced. Drilling data was often a diagram or plot of the circuit image, with letter codes placed beside hole locations to signify hole size.

The wide use of vector photo plotters had a significant, but not revolutionary, effect on the front-end of PWB manufacturing. These plotters, for the most part now obsolete, consisted of a light source, aperture wheel, and moving table. Film was exposed trace by trace. Rather than creating artworks, 1-1 film plots were generated and the reduction step eliminated. Vector plotters were generally too slow to be employed for imaging large, step-and-repeated, ready-to-use photo-tools. For example, an 18 x 24-inch image could have taken several hours per layer to plot on a vector plotter. Therefore, PWB shops were still required to manually create photo-tools by making contact prints of the photo-plotted original and registering them to the hole pattern of a drilled panel.

Personal computing equipment, inexpensive circuit layout software, and laser photo plotters have eliminated manual methods of circuit layout. Currently, virtually all circuit layout is done on computers and the output—image files—are sent to laser photo-plotting service bureaus or PWB shops with laser photo plotters. Since these machines are much faster than their vector predecessors, it became practical to manipulate the image data (and the associated drill and route data) prior to photo-plotting. CAD software became available and performed simple editing of image files, such as step-and-repeating, adding borders, vents, or text—even adding, changing, or deleting circuit features. The image file sent to the photo-plotter would return as a ready-to-use photo-tool.

In the modern PWB shop, data is received by modem or magnetic media. The circuit image files (usually "Gerber" files, so named for the company that created the format for its vector photo-plotters), along with drill and route programs, are displayed for sales, quoting, and overall manufacturability purposes. Thereafter, the image files are manipulated and edited to produce the image files for a customized photo-tool. The department responsible for this data processing, usually referred to as the CAD department, may also perform design checks and other engineering functions. Higher-end software packages include design-rule check modules to automatically search the image and drill files for violations such as power-to-ground shorts, trace and space widths or annular ring sizes.

B. Inner Layer Image Transfer

1. Overview

The function of this large use cluster is to transfer an image of a circuit layer from a film photo-tool (or directly from data, in the case of direct imaging) to the copper foil of PWB base laminate (Figure 2-5). Two basic strategies, subtractive and additive, exist. Subtractive inner layer image transfer is accomplished through a series of processes that together are referred to as "print-and-etch," and is by far the predominant method. Additive methods of multilayer circuit manufacturing are covered in Section I.C.6—therefore, only one broad technology exists in this cluster. Several secondary clusters exist within this use cluster—one is associated with imaging. Direct imaging looms as a major advancement to conventional photo-tool imaging, but has failed to make significant inroads.

Etching is another secondary cluster with two major chemistries as alternatives. Inner layer base material selections can be made that eliminate some of the wet processing in this cluster. We have included in this cluster steps not generally thought of as part of image transfer. These include the material preparation processes of shearing and surface cleaning, photo-plotting, and oxide treatment. In each case it will be seen that specific print-and-etch regimes can be employed to eliminate one or all of these steps making their inclusion logically desirable.

2. Conventional Print-and-Etch

Print-and-etch is a series of process steps that accomplish the goal of image transfer for inner layers from photo-tool to copper (print-and-etch may also be used for outer layers, although complicated somewhat by the need for through-hole plating). During the "print" step, photoresist is applied to the surface copper of PWB material. Photoresist is a light-sensitive organic coating that can be imaged with a photo-tool and a light source. When exposed and developed, the circuit image is transferred to the photoresist (Figure 2-6). During the etch step, copper that is not protected by the photoresist (which now becomes the etch-resist), is etched away and only the image of the circuit remains. The photoresist is then stripped, revealing the copper circuit remaining beneath it. Print-and-etch is a subtractive process—there is much less copper on the layer after the process than before.

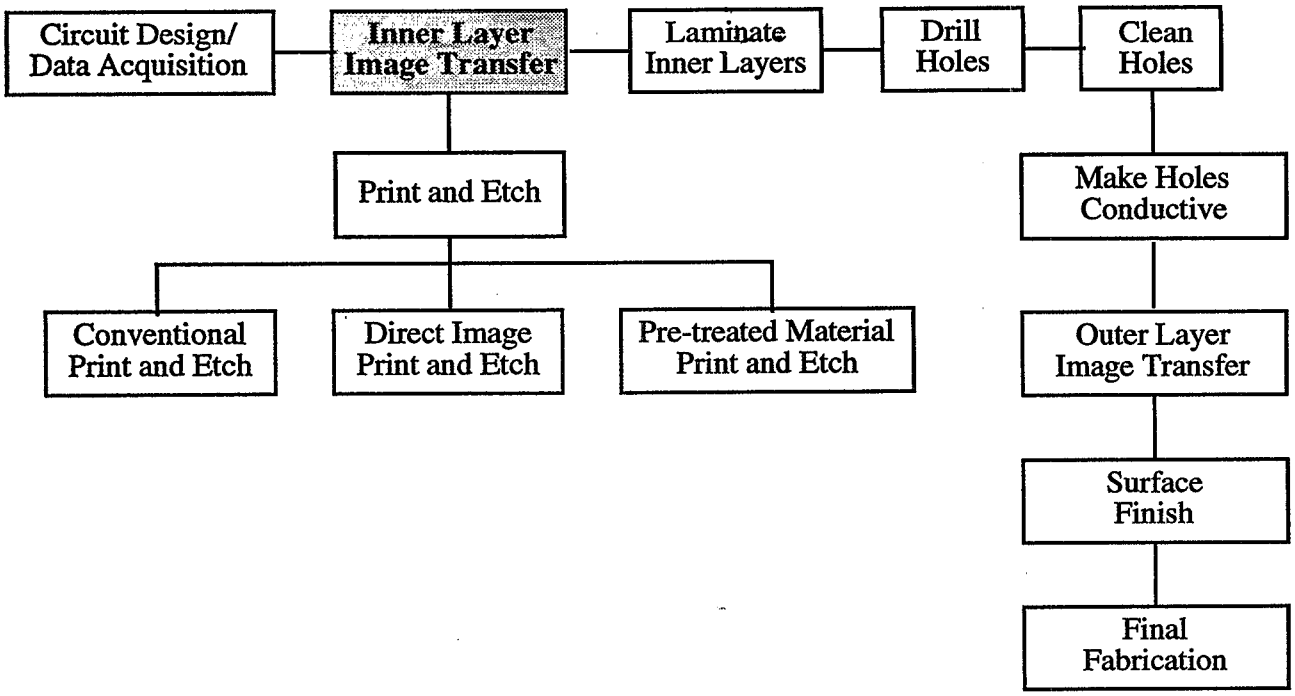

Figure 2-5. Inner Layer Image Transfer Use Cluster.

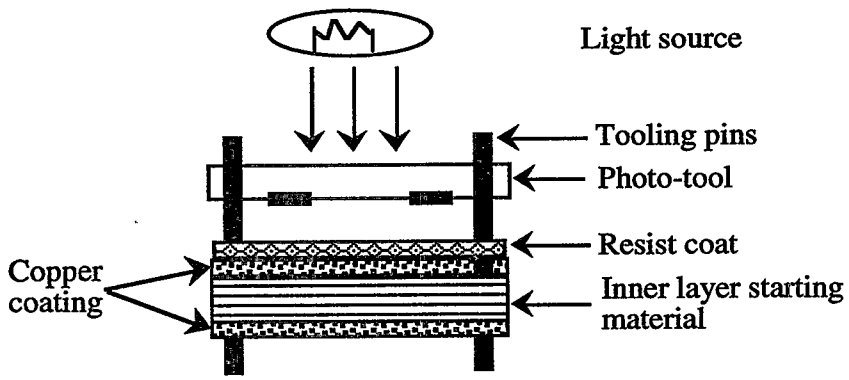

Figure 2-6. Schematic Drawing of an Exposure Tool for Inner Layers.

a. Photo-tool Creation

Image transfer begins with photo-tool preparation. The photo-tool functions like a negative in photographic printing—the image of the circuit is created on the photo-tool. A photo-tool is usually a film image (the film may be mounted on glass or the image transferred to glass) of the circuit layer. It is placed between the light source and the resist-coated panel during the exposing (or printing) process. The line drawn between data acquisition and photo-tool creation is blurred by the fact that photo-tools are "created" virtually at computer workstations, then physically by laser photo-plotters. Prior to the widespread use of laser photo-plotters, photo-tool creation was largely a conventional photographic process handled by the graphics arts (or "camera") department. This department,

now obsolete, was responsible for photo-tool creation. Now, photo-tools are laid out by the CAD department, then photo-plotted.

Presently, all PWB shops have in-house laser photo-plotting or have access to laser plotting service bureaus. Furthermore, concurrent with the advent of laser photo-plotting has been the development of inexpensive CAD software. Complex manipulation of image files, such as rotation, mirroring, or the addition of vents, identification marks, tooling marks or targets, and so on, is done on computer workstations in the CAD department. The resulting photo-plots may be directly used as photo-tools for initial production runs. Film developing is usually done in a three- or four-chambered conveyorized developer that includes developer, stop, fix, and drying steps. Silver is present in the small amount of waste water generated. The presence of silver necessitates a method of silver removal (since this waste stream is regulated), although most shops do not approach the limit in their combined waste stream since the total mass of silver discharged from this one process is very small.

Film photo-tools are usually precision punched to match holes punched in the interior layers of the PWB or to match tooling pins preset in exposing frames. Tooling regimes vary from shop to shop but all are designed to preserve layer-to-layer registration. Film photo-tools are inspected for defects by eye or by automated optical inspection devices. These machines are capable of flagging defects in the plotted image due to handling, dust, or other causes.

b. Material Preparation

The PWB base material, or "laminate," consists of a dielectric material sandwiched by copper foils. Both the copper foil and the dielectric core are manufactured in various sizes. Foil thickness is stated in ounces/ft^2. Core thicknesses range from 3 to 47 mils (1 mil = 0.001 inches) for inner layer manufacture. Most PWBs are manufactured on glass-woven epoxy-based materials, with the most common resin system being FR-4 (flame retardant-4). Other materials are selected for specific electrical, physical, performance, or cost characteristics. Two examples of alternative materials include: high-temperature stable/low-dielectric constant polyimide and very low-cost phenolic paper. The core material is sheared to panel size, then cleaned mechanically, chemically, or by a combination of both. The purpose of this cleaning step, referred to as "pre-clean" or "chem-clean" is to remove surface contamination, including any anti-tarnish coating present and to condition the surface copper topography so as to promote the subsequent adhesion of photoresist.

Mechanical scrubbing methods include abrasive brush scrubbing and pumice scrubbing. Brush scrubbing removes a thin layer of surface copper, thus ensuring a clean surface, but tends to impart stress to thin core material by deforming it during the scrub. Brush scrubbing can also produce a surface not compatible with fine-line circuit designs. Pumice or aluminum oxide scrubbing imparts less or no stress to the material and produces a favorable surface for photoresist lamination, but is known to be ineffective at removing anti-tarnish coatings applied by laminate manufacturers. Thus, pumice scrubbing is often accompanied by at least some chemical cleaning components.

Chemical cleaning is usually accomplished in a conveyorized spray chamber. Two chemistries are sprayed onto the surface of the panel. The first is usually a proprietary product designed to remove anti-tarnish coatings. The second is a micro-etchant such as potassium persulfate, which is applied to further clean the surface and leave a desirable surface finish. A third chamber may include a mild anti-oxidizer.

A minority of shops have eliminated the cleaning step by purchasing pre-treated material, often referred to as "double-treat" material. The laminate is purchased with an oxide coating already present and the sheared panels (the laminate may be purchased already sheared to panel size to reduce handling)

are immediately ready for resist application. While this laminate is generally more expensive, two wet processing steps are eliminated (cleaning and oxide). Lower discharge and fewer process lines make this alternative attractive, especially to smaller shops. Although economies of scale are realized when material manufacturers treat the surface copper, the overall efficiency of this alternative is clouded by the fact that most of the surface copper on an inner layer is etched away. Thus, most of the resources spent treating the surface copper prior to etching is wasted. Ultimately, the solution to this problem could focus on reducing the amount of materials put onto the laminate temporarily. For example, direct imaging of copper could reduce the need for copper etching. Double-treat material is not used on outer layers because the oxide coating on the copper lines prevents the deposition of nickel, gold and solder onto the copper circuitry. These metals are required for assembly.

c. Imaging

The term "imaging" usually refers to three process steps: photoresist coating (sometimes referred to as "lamination"), exposing (or "printing"), and developing. When completed, the panel is ready for etching, with the imaged photoresist now ready to act as the etch-resist. The most common photoresist in use today is dry film. Prior to the rapid conversion to dry film, which occurred in the early 1980s, etch-resists were screened onto panels. The performance benefit and ease of use of dry film ensured the virtual revolution. Other photoresist schemes exist—liquid resists can be sprayed or applied by dipping, or even electrostatically deposited. The continuing improvement of dry film performance (0.003-inch traces and spaces are routinely achieved with various dry films) has, however, left little room for the alternatives. Furthermore, modern dry film resists for common print-and-etch functions are fully aqueous and are developed in a simple carbonate solution.

Dry film photoresists can be purchased in a variety of thicknesses, ranging from less than 1 to 3 mils, and a range of products with subtle performance differences are available. Dry film resist is typically packaged in rolls and is applied with heat and pressure to the surface of the panel, usually with a hot roll or cut-sheet laminator. The photo-polymer film layer is sandwiched between a separator sheet that is automatically peeled away by the lamination equipment, and a mylar cover sheet, which may remain atop the resist layer until development when it is removed by hand. Dry film used by the PWB industry is negative-acting film, i.e., that portion of the resist layer which is exposed to an appropriate light source will polymerize and will not develop, whereas the remaining areas of resist will remain soluble and develop away in a suitable developing solution. Thus, the photo-tool for inner layer print-and-etch should be a negative film; the circuit area should be transparent to light, while the non-circuit areas should be opaque. This will result in a resist image of the circuit remaining atop the copper layer after development.

Exposure (printing) is accomplished by placing the panel and its photo-tools in a vacuum frame and directing a light source for the appropriate time at the panel. Exposing equipment consists of one or two light sources and a drawer that holds the vacuum frame. Numerous photo-tool registration strategies exist. The most common is to mount the top and bottom photo-tools onto a glass frame that can be adjusted to bring the two layers into registration. Panels are placed into the frame, which is then closed, a vacuum is drawn, the light source is switched on, and both sides of the laminate are exposed simultaneously.

The development of fully aqueous film resists is performed in a warm sodium or potassium carbonate solution. Concentrations of less then 2% are common. Developing is done in conveyorized spray chambers that have a developer module along with one or more rinse modules. Both sides of the laminate are developed together. The use of semi-aqueous or solvent-developing dry films is no longer common for any application and is very rare for inner layer parts. The spent developing solution,

which contains the carbonate and dissolved resist, is one of the largest (in terms of volume) spent process fluid waste streams in the PWB shop.

d. Etching

Panels approaching the etcher have exposed copper and a resist image of the circuit pattern. Etchant, sprayed onto the surfaces of the panel, removes the exposed copper, but cannot significantly dissolve the copper residing under the resist. In this way, a copper circuit is formed. Etching is performed with conveyorized equipment that typically includes a main spray chamber, an etchant flood rinse, and several cascading water rinses. Long conveyorized units that include developing, etching, and film stripping are common only in large production shops. Acidic cupric chloride and alkaline ammoniacal are the most common etchants (sulfuric-peroxide, a common microetchant, is also employed as a primary etchant). Chromic acid and ferric chloride, dominant in the past, are now rarely found. A complex array of issues surround the choice between the remaining chemistries, and the decision is tied to downstream process material choices as well as economic considerations.

For example, cupric chloride is generally incompatible with the metallic resists (tin or tin-lead) which are commonly applied to outer layers, but may be selected for inner layers based on performance (for fine-line etching), pollution prevention (ease of on-site regeneration and copper recovery), or other issues. In this example, two etching systems are required, cupric chloride for inner layers and ammoniacal for outer layers. Etching, a one-step conveyorized process, is not often a production bottleneck and two etching systems may be difficult to justify. For this reason, many small shops employ the more versatile ammoniacal etchant for both inner and outer layers. Cupric chloride etchants consist of cupric chloride ($CuCl_2$) and hydrochloric acid. The simple etch reaction is driven by copper's two oxidation states:

$$Cu + CuCl_2 \rightarrow Cu_2Cl_2$$

Since no metal complexer is present and the reaction is reversible chemically by chlorination, oxidation with peroxide or other oxidizer, or electrolytically, cupric chloride is far easier to regenerate on-site than ammoniacal etchants. Several closed-loop regeneration systems have been developed that reoxidize cuprous chloride and maintain total copper content at desirable levels (usually in the 15 to 20 ounce/gallon range). Chlorination, the most common method, is performed in a closed-loop arrangement in which spent etchant is circulated through the chlorinator and back to the etcher sump. Copper oxide waste is produced. Furthermore, since this etchant is acidic, no attack on the alkaline-sensitive dry film resists occur. Cupric chloride has a similar etch rate to ammoniacal but is not, as mentioned above, compatible with many metal resists.

Ammoniacal etchant is popular due to ease of use and general compatibility with most resists. Ammoniacal etchant systems are comprised mainly of ammonium hydroxide and ammonium chloride. Other ingredients are present to a lesser degree and serve a variety of functions. As with cupric chloride etchant, the etching reaction is driven by the cupric (Cu^{++}) ion:

$$Cu + (Cu(NH_3)_4)^{+2} \rightarrow (2Cu(NH_3)_4)^{+1}$$

Ammoniacal etchants are maintained for continuous operation with a feed-and-bleed arrangement based on baume or specific gravity measurements. In this arrangement, a pump is connected to a baume-activated switch. When the baume of the etchant in the sump rises due to the increasing copper concentration, the pump is switched on. Copper rich etchant is removed from the sump while fresh etchant is introduced. In this way, a steady concentration of copper (critical in maintaining a steady etching rate) is maintained. Spent ammoniacal etchant is not commonly regenerated or recycled on-site,

rather, it is usually pumped into barrels or tanks and shipped off-site for recycle and metal recovery. At least one ammoniacal etchant regeneration system, based on solvent extraction, is commercially available for on-site regeneration. The system incorporates electrolytic copper recovery in addition to etchant regeneration. The spent ammoniacal etchant stream is the largest stream shipped off-site by PWB shops.

e. Resist Stripping

After etching, film stripping is performed. Stripping may be done in-line with etching as simply another spray chamber at the end of the conveyorized etch line or in a tank. For dry film resists, a wide array of strippers exist. The simplest is hot potassium hydroxide (KOH). Simple aqueous strippers tend to remove resist in strips that do not fully dissolve, making them generally inappropriate for spray operations. Monoethanolamine (20% by volume in an alcohol solvent) is frequently the chemistry of choice for many applications. Other proprietary formulations abound. Methylene chloride is declining in use, and is unnecessary for fully aqueous films.

f. Oxide

Oxide treatment, common in the plating industry as a paint base, is used in PWB manufacture to promote copper-to-epoxy adhesion in multilayer manufacture. The oxide process line usually contains four or five process tanks and three or four rinse systems (Figure 2-7). The process tanks consist of a hot alkaline cleaner, a micro-etch, and the oxide bath itself, which may include a dilute pre-dip for drag-in protection. The micro-etch may be persulfate- or peroxide-based. Oxide chemistries are usually proprietary—a common oxidizer is sodium chlorite with sodium hydroxide. Other ingredients vary from vendor to vendor. The oxide bath must be quite hot, usually 140 to 150°F or hotter. The process takes 15 to 30 minutes to complete.

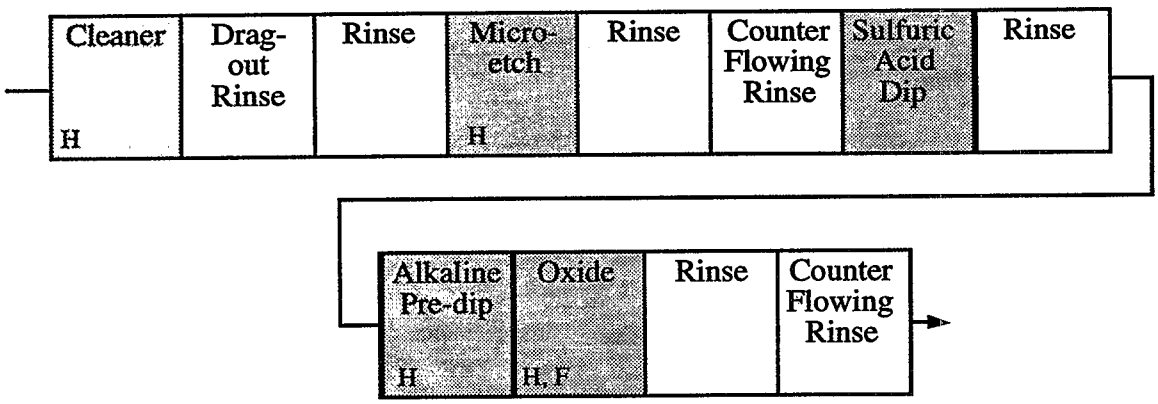

Figure 2-7. Typical Oxide Process Line.

3. Image Transfer Options

a. Direct Imaging

There are two approaches to direct imaging, an option that eliminates the need for photo-tooling. In the first approach, the inner layer is coated with photoresist as in conventional imaging, but the pattern is generated by direct exposure of the resist with a laser rather than through a patterned film. In the second approach, no photoresist is applied. The dielectric layer is coated with a

bound plating catalyst material that is photo-sensitive (either positive- or negative-working). For a positive-working actinic catalyst, ultraviolet (UV) light in the presence of an aromatic diazo compound and cupric acetate is used to reduce the Cu^{+2} ion to its metallic state. Unexposed areas remain non-conductive. (This process is described in further detail in Section I.A.7, Additive Metallizations.) Further plating can be done using some form of electroless plating to build adequate copper thickness. Because the sidewalls of the resulting metal lines are unconstrained in this process, there are design limitations to this option. This process has been successfully demonstrated on ceramic materials.

Direct imaging plotters have been available for a decade or more, but few shops currently employ this method. High capital costs for direct imaging equipment are a barrier for medium to small shops. Furthermore, exposure times are 2 or 3 times longer than with conventional imaging. Ironically, it is the prototype manufacturers, least able to make purchases of this magnitude, that could benefit most from this technology. Film usage in prototype shops is much higher per unit of manufactured PWBs than in large production houses (where a single photo-tool may be used to expose hundreds of panels), and in some cases, prototype manufactures may be able to better tolerate the longer print times.

In addition to the potential cost-savings in a high-mix, low volume shop, elimination of photo-tools may also increase yields in all shops by improving alignment between layers. Film photo-tools suffer from dimensional instability and great care and expense are required to control the environment of the plotting and print area. Film stretch (or shrinkage) may reach several mils in the corners of 24-inch photo-tools and in many cases it is the largest contributor to the overall registration tolerance of the manufacturing process. With direct imaging, only the positional tolerance of the imager (usually claimed to be under 1 mil over 24 inches) contributes to misregistration.

b. Pre-treated Materials

Post-metal etch oxide treatment can be eliminated by purchasing material that is already oxidized or otherwise treated (such as double-treat copper). An oxide line consumes considerable energy and water and can include as many as 12 to 15 process and rinse tanks (if all of the rinse systems are two-stage counterflowing). Obviation of this process step is particularly attractive to small or quick-turn prototype shops. On the other hand, pre-oxidized material may be eliminated as an option in some shops that use automated optical inspection (AOI) to search for defects. The oxidized copper surface, black or dark brown in color, is unacceptable for many AOI units that depend on reflected light.

C. Lamination

Lamination is the process of putting together the various layers. While some variety of materials (such as release sheets) exists, this process is quite uniform between manufacturers. Some production shops have used off-site lamination of 4- and 6- layer boards, enabling them to produce multilayer circuits without investing in lamination and other multilayer equipment. As higher layer counts have become more common, most shops have been forced to create in-house multilayer lamination departments, including lamination presses, oxide and desmear pressed lines, and other multilayer-lamination departments.

Lamination may be divided into several steps. First, the multilayer inner layers and ancillary materials are assembled in a stack in preparation for lamination. At this point, the circuit patterns have been generated on each layer of copper/dielectric laminate. The stack is held in registration by tooling pins. A typical circuit stack will include copper foil, B-stage (substrate material with semi-cure epoxy, also referred to as prepreg) and the etched inner layers. B-stage styles are selected to provide the multilayer circuit with the specified overall thickness, and several sheets may be placed between successive

inner layers. Several circuit boards may be pressed in one stack or "book" and they are separated by coated aluminum sheets or other release materials. Cleanliness is essential during the lay-up operation; however, not all manufacturers perform this process in a cleanroom environment. Dust and other contaminants can degrade the bondline between copper and epoxy.

During the press cycle, heat and pressure are applied. Modern presses have platens that are enclosed in a vacuum chamber, because vacuum greatly enhances overall performance by removing air and volatiles from the panels as the B-stage cures. Press cycles are usually computer-controlled. The specific cycle is dictated by the substrate employed; for FR-4, temperatures of 350°F (≈176°C) and pressures of 150 to 350 psi are common, and the cycle requires more than 1 hour to complete. Press platens may be heated with stream or electricity.

D. Drilling

1. Overview

Vias (holes drilled through a PWB for the purposes of layer-to-layer interconnection) are drilled into the PWB to connect the inner and outer layers (Figure 2-8). The etched copper pattern of the inner layers extends to certain hole locations. After drilling, the inner layer foil extends to the barrel of the hole and is available for interconnection when the hole barrel is metallized. This drilling of PWBs is performed almost universally with computer numerical control (CNC) drilling equipment and tungsten-carbide drills. Most variation between manufacturers occurs in the selection of entry and back-up materials, where a number of options exist—these are discussed below. Laser ablation, an alternative drilling technology, has generated considerable interest. Laser ablation is particularly good at removing organic materials but removes copper at a much slower rate.

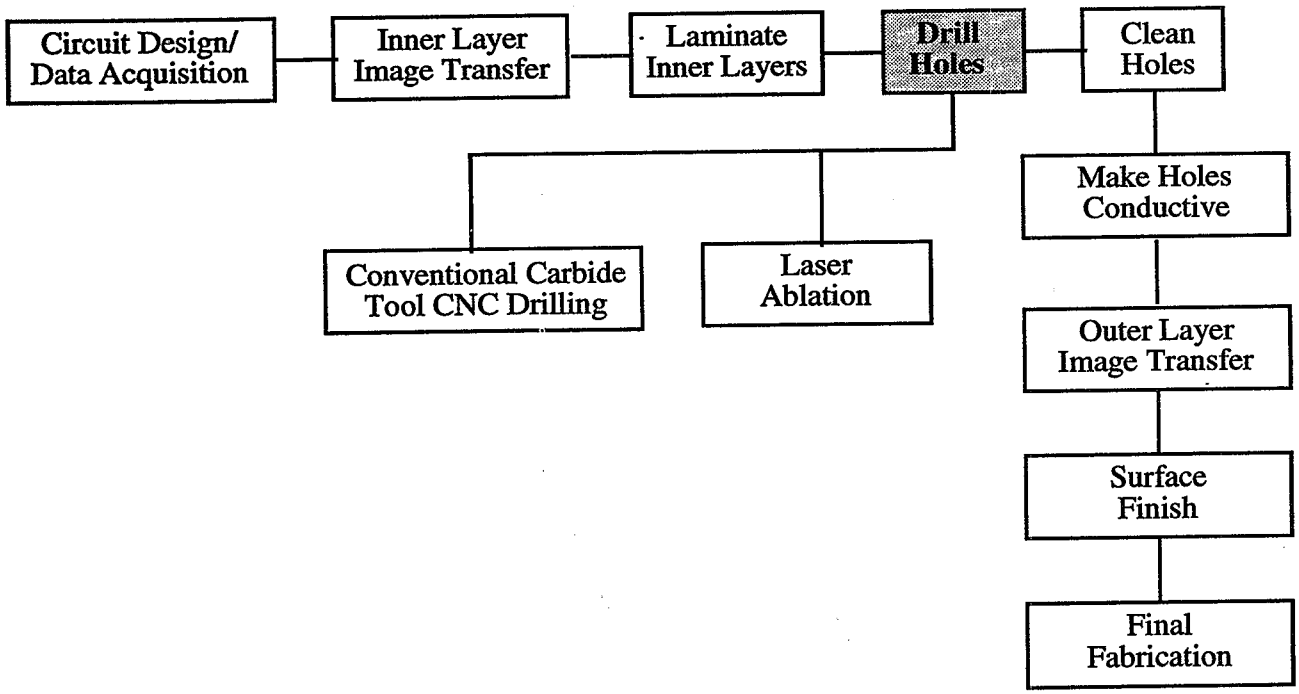

Figure 2-8. Drill Holes Use Cluster.

2. Conventional CNC Drilling

a. Introduction

Common CNC drilling equipment consists of a table, which moves along two axes, and one or more drill spindles that move in the z-axis. The machine is controlled by a computer that reads a list of commands referred to as the drill program. These programs are created, nearly ready to use, by circuit layout software and are then step-and-repeated along with the image files for optimum panel usage. Basic commands found in all drill programs direct the machine to move the table to a specified location, cause the spindle assembly to drill a hole, or effect a tool change. Other commands set the "feeds and speeds" or the vertical and rotational speed of the drill as it enters and exits the PWB material. In operation, the drill machine will drill holes at a rate of a few per second, depending on the distance between the consecutive drilled holes and the entry, and withdrawal speeds of the drill. High-end CNC drilling equipment include features such as large tool trays that hold 100 or more tools and facilitate automated tool-use management, broken tool detection, automatic stacking, loading, and unloading.

b. Entry Material

The top layer that the drill enters before PWBs are drilled is called "entry material." The PWBs are drilled in stacks that consist of a sheet of entry material, one or more circuit panels, and back-up or exit material. Entry material is required to reduce or eliminate exit burring and to reduce drill wander, which is the tendency of the drill to briefly skate on the surface before penetrating. A variety of entry materials exist. The most common are paper-phenolic (10 to 24 mils thick), paper-melamine (10 to 24 mils thick), aluminum (7 to 15 mils thick), and an aluminum-clad material consisting of a phenolic, melamine, simple paper, cellulose, or other core. Entry material is discarded for recycle or disposal after use.

c. Back-up Material

The drill bit terminates its downward stroke with the point penetrating the back-up material in order to complete the drilling of the bottom panel in the stack. Back-up materials are generally 0.062 or 0.093 inches thick. Common materials are pressed wood products (pulp or fiber), paper-phenolic-clad with a wood product core, or aluminum-clad with a wood product core. Since the drill penetrates only halfway through back-up material, it is generally flipped over and used a second time before being discarded.

d. Drill Bits and Process

Drills used by the PWB industry range in size from 0.005 to 0.250 inches in diameter. As circuit densities have increased, hole sizes have decreased in an effort to conserve space. Common via sizes today are in the 0.015 to 0.025 inch range, while the leading technology is demanding considerably smaller holes. The basic improvement in conventional drilling equipment to accommodate the small hole demand has been the air-bearing spindle, which is capable of the high rotational speeds (greater than 100,000 rpm) demanded by the delicate small tools. New drills are capable of 1000 to 5000 hits before becoming unacceptably dull. Drills are usually resharpened 2 to 4 times before being discarded.

3. Laser Ablation

Lasers can be used as an alternative to mechanical drilling to form holes (vias). They are especially well-suited to blind via formation—when a via is drilled from the surface of a PWB that terminates within the substrate to provide interconnection for some, but not all, of the layers of a multilayer PWB—but can do a very good job at through-hole and buried via formation. Buried vias are drilled through the inner layers prior to lamination and provide interconnection for a pair of inner layers (such as layers 2 and 3 of a 4-layer PWB)—when the PWB is laminated, the via is buried by the surface layers. Research has been done in blind via formation by groups researching MCMs at IBM and MCC[9] as well as by equipment vendors such as Litel and ESI. Table 2-1 shows some of the different laser drilling options and their respective advantages and disadvantages.

Technique	Advantage	Disadvantage
CO_2 laser	Low equipment cost	Minimum geometry limited by wavelength to >30 μm, thermal ablation requires cleanup, serial drilling process (one hole at a time).
IR/Argon Ion/Nd:YAG laser	Low equipment cost, smaller features than CO_2	Serial drilling process (one hole at a time), requires cleanup.
Frequency quadrupled YAG laser (UV wavelength)	Modest equipment cost, small features possible	Frequency quadrupling not robust, serial drilling process (one hole at a time).
Excimer shadow mask	Small features possible	Low throughput (most energy wasted), need for *in situ* masking, laser sources expensive.
Excimer projection (Litel Instruments)	Small features possible, high throughput, simple optics	Expensive laser, large features difficult, potential via density limitations.

Table 2-1. Lasers Available for Via Formation in PWB Fabrication.

Because of the intriguing cost-performance potential of the Litel projection technique relative to other options, MCC's efforts were focused on demonstration of projection excimer (short wavelength/ high energy) machining in MCM applications. The Litel technique involves proprietary tooling that serves to concentrate a flood illumination excimer beam source to the areas requiring machining. Shadow mask techniques reflect back laser energy from all areas but the features (vias) to be machined. Since for most applications the net via area is small compared to the part, the majority of the excimer energy is lost and throughput is very low. In contrast, the Litel technique collects energy spatially and concentrates it at the areas to be machined, vastly improving energy density at the surface and improving throughput dramatically. In addition, non-contact tooling is used with the Litel approach rather than either contact tooling or *in situ* masking characteristic of the shadow mask approach. Because of the proprietary nature of Litel's technique, further details of the approach should be acquired from Litel.[10]

MCC and Litel did a series of experiments to explore the use of lasers for drilling laminate materials. In the first experiment, an array of greater than 100,000 vias having diameters less than 1 mil (<25 μm) and spread over an area less than 10 sq. inches were drilled simultaneously in a spin-coated

9 D. Carey, M. Breen, et al., "Low Cost Interconnect 1 Final Report," MCC Technical Report #HVE-161-92(Q), pp. 127-130.

10 San Diego, CA, Phone: (619) 546-3788.

high-temperature thermoset plastic dielectric material. The pitch was as small as 2 mils. Researchers found that:

Positive

- Drilling of all holes was finished in less than one minute.
- Vias of less than 1 mil diameter were fabricated on a 2-mil pitch (one via of 1 mil diameter every 2 mils of linear spacing). This is good for high density interconnect.
- Via placement was accurate over the whole drilling area.

Negative

- Stray energy from the laser created surface damage in the areas adjacent to the via areas.

A second experiment was done to investigate the applicability of laser drilling for high-end PWBs. In this experiment, several thousand 2- to 3-mil diameter holes were drilled simultaneously in a 1- to 2-mil thickness of polyimide film (Upilex®). The design chosen for the experiment had two layers of circuitry in the x-y plane and two via layers (connections normal to the z-axis). The vias were larger and more widely spaced than in the previous experiment.

Both wafer and laminate samples showed excellent results. Holes were accurately machined on-center (locally) and corner to corner (globally) over the sample area. Drilling took less than 30 seconds per site in the second experiment. According to the MCC technical report, standard drilling costs are approximately 0.5 to 1.0¢/hole. Laser drilling has the potential to lower drilling costs substantially (capital + labor + materials).[11] In addition to the potential cost benefits, laser drilling could have environmental advantages over mechanical drilling. Since vias can be accurately placed and their dimensions controlled, the routing density per layer can be higher. In many cases, this would allow manufacturers to achieve the same level of connectivity with fewer layers and the associated environmental costs.

E. Hole Cleaning

1. Overview

Hole cleaning generally refers to a process called desmear and/or the closely related process of etchback (Figure 2-9). Desmearing holes refers to the removal of a small amount of epoxy-resin from the hole barrel—including any that may have been smeared across the copper interface during drilling. The smear on the copper surface, if not removed, would prevent interconnection between it and the electroless copper which is to be plated in the hole barrel. Etchback, performed less frequently on standard materials due to the advances in the performance of desmear chemistries and the subsequent relaxation of most specifications, is the removal of a significant amount of epoxy-resin and glass fibers (as much as 1 to 3 mils) that leaves the copper interface protruding into the hole. The protruding copper surface allows a large surface area for the interconnection with the subsequent copper plating and the surfaces exposed by the removal of epoxy cannot have been smeared during drilling. Most of the demand for etchback stems from military specifications. The necessity, even the advisability, of a 3-mil etchback has been frequently called into question and, for the most part, specifications covering this process have been relaxed.

Deburring and scrubbing are processes performed immediately prior or after desmear or etchback. During drilling, copper burrs may be raised on both sides of the panel by the action of the drill entering

11 D. Carey, M. Breen, et al., "Low Cost Interconnect 1 Final Report," MCC Technical Report #HVE-161-92(Q), pp. 23 and 127-130.

and exiting the material. The burrs are sanded smooth on a deburring machine, which consists of a sanding wheel and a conveyor. In wet deburrers, copper dust is carried off in a waste stream. Dry machines usually are outfitted with vacuum units. Deburring is more correctly considered a surface preparation step rather than hole-cleaning. Scrubbing is performed as a surface preparation step prior to electroless copper (and during other stages, such as before solder mask). Scrubbing may be performed similarly to deburring except a much less aggressive surface abrasion occurs. Pumice or aluminum oxide scrubbers, which direct a high-pressure spray of abrasive particles at the PWB are also used for surface preparation.

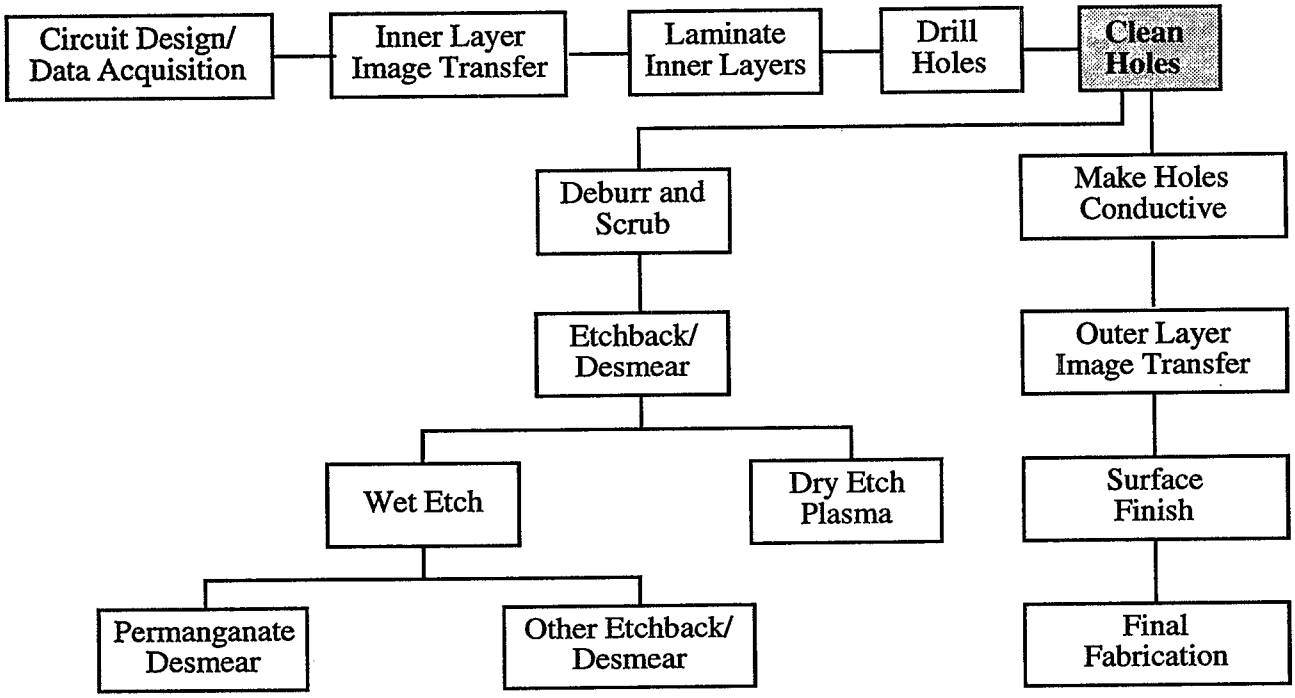

Figure 2-9. Clean Holes Use Cluster.

This cluster has seen considerable change over recent years. Wet chemical methods have been refined and permanganate seems to have been settled on as the desmear oxidizer of choice. Electrolytic regeneration systems are now commonly applied to permanganate baths to greatly extend their life and make overall control of the process quite simple. Plasma desmear/etchback has become a common alternative. Originally, high capital costs proved to be a barrier for wide acceptance of this technology. Used equipment and the availability of somewhat less expensive models have increased overall use. Also driving the popularity of plasma desmear/etchback is the elimination of the wet process line otherwise required, and the fact that it can produce both epoxy-resin and glass etchback.

2. Wet Chemical Desmear and Etchback

a. Wet Chemical Methods

Currently, the most widely used chemistry is sodium or potassium permanganate when significant etchback is not required or specified. Permanganate-based systems remove a thin layer of epoxy-resin (typically less than 1 mil) and smear and are quite adequate for desmear-only applications.

The permanganate desmear line consists of three process baths (Figure 2-10). The first is a solvent conditioner designed to swell and facilitate the subsequent removal of the epoxy-resin smear. The constituents of this bath are usually proprietary, some include n-methyl pyrrolidone (NMP). The second bath is usually the permanganate itself. The make-up is 8 to 10 ounces/gallon of permanganate in a sodium hydroxide solution. The bath is generally heated to 160°F or higher. Concentration, temperature, and dwell time are all varied to arrive at an optimum epoxy removal. Dwell times are quite long—20 minutes or more is not uncommon. By-products, consisting of the reduced manganate ion (MnO_4^{-2}) and other manganese compounds, develop rapidly in the heated bath and are usually removed by filtration. Frequent analysis and permanganate adds are necessary. Electrolytic regeneration units, consisting of a ceramic porous pot, cathode, anode, and rectifier, have been developed and are designed to anodically re-oxidize the manganate ion back to permanganate (MnO_4^-). These units can be calibrated to effect a steady concentration of the permanganate ion over long periods of time, eliminating the need for frequent analysis while reducing sludge formation and extending overall bath life. The final bath is a neutralization step, designed to remove permanganate from the holes and surface of the panel. Sulfuric acid based chemistry is common.

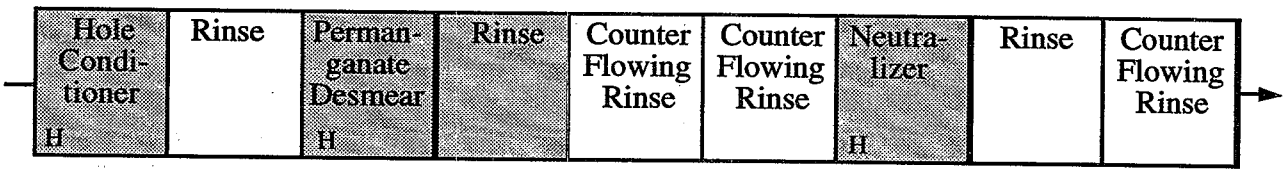

Figure 2-10. Typical Desmear Process Line.

Other systems have been largely discarded for various reasons. Originally, chromic acid was the chemistry of choice, but health and waste disposal issues have eliminated it as an option.

Concentrated sulfuric acid (usually 93%) is still in use, but generally requires a permanganate step for final hole cleaning, making it a significantly longer and more expensive process than permanganate alone. It still finds application, however, when etchback is required because it is more aggressive than permanganate and it remains as the only viable wet chemistry option. Handling the concentrated acid and operation of the line has proved to be a problem in many shops. The amount of epoxy-resin removal is controlled by the dwell time in the sulfuric bath, which must be precisely monitored. Sulfuric acid does not etch glass, however, and a second step is required to perform the glass fiber etch. Glass etchants include hydrofluoric acid (rarely used), hydrochloric acid, and ammonium bifluoride.

b. Plasma Etchback

Plasma etchback can be used to remove both epoxy resin and glass. By varying the parameters of the etch chamber, responses such as etch rate, throughput, and selectivity of glass fiber to epoxy etch can be controlled. The cost of plasma etch systems appropriate for PWB applications could be below $100,000 for certain applications. Very little process gases are used in the plasma etchback process [typically 100 standard cubic centimeters/minute (sccm) or ~400 gallons/day running at 100%]. In the integrated circuit fabrication industry, it is common practice to vent these unregulated inert gases to the atmosphere, although in some cases they are scrubbed with other gases. Inside the etch chamber, plasma etching is a six-stage process including the following steps:

- Forming reactive species,
- Transferring reactive species to PWB surface,
- Adsorption,

- Reaction,
- Transferring reacted species away from PWB surface, and
- Removal of reacted gases from process chamber.

Critical parameters for the etch process include: etch gases, chamber power, pressure, and gas flow rate. Table 2-2 shows where some of these parameters might be set:

Parameter	Epoxy Etch Settings	Glass Etch Settings
Etch gas	O_2, $O_2 + CF_4$, $O_2 + SF_6$	CF_4, SF_6, $O_2 + CF_4$, $O_2 + SF_6$
Power	200 to 2000 Watts	200 to 2000 Watts
Pressure	200 to 1500 mTorr	200 to 1500 mTorr
Flow rate	10 to 200 sccm	10 to 200 sccm

Table 2-2. Plasma Etchback Parameters.

Oxygen is required to etch organic materials like epoxy or polyimide. It also increases the etch rate of glass when combined with fluorine-containing gases. Plasma etching can be done on multiple substrates either as a batch process or on one substrate at a time. Batch processing can usually be completed in a few minutes; however, etch uniformity is usually somewhat better on substrates that are processed one at a time. Large substrate size is not a fundamental problem, but increasing the chamber size also increases equipment cost. Etch rates between 0.1 μm to 1.0 μm/minute are typical. CF_4 with O_2 are commonly used to simultaneously etch glass and epoxy. Possible by-products from this process include some fluorocarbon molecules.

F. Making Holes Conductive

1. Overview

For holes to serve their intended purpose of creating layer-to-layer interconnection, they must be coated, or plated through with a conductive substance (Figure 2-11). Since PWB substrate material is not conductive, electroplating copper directly to the substrate is not possible. First, a seed layer of copper or other conductive material must be plated or coated onto the hole walls, or barrels. After the seed layer is applied, electroplating of a relatively thick (0.001") layer of copper is possible.

The next step in PWB fabrication is to provide electrical connection of the various layers of the PWB through the holes created during drilling or laser ablation. We have called this part of the process "making holes conductive." This is accomplished by depositing metal along the sidewalls of the holes (vias). This is usually done with electroless copper plating. Other methods that may offer improved cost and environmental performance are emerging to challenge the existing practice. Until the latter half of the previous decade, all shops were using electroless copper to metallize hole barrels and create the interconnect between circuit layers. The general strategy has been to plate a thin layer of electroless copper to make the conductive surface that is required for electrolytic copper plating. This mature technology has produced reliable interconnects for decades. However, the industry has sought alternatives to electroless copper, and this search intensified during the 1980s. While none of the chemistries present in the electroless copper line are particularly expensive (with the possible exception of the palladium-based catalyst), the typical line is long (17 or more tanks, depending on rinse configurations) and may have 8 or more process baths. The electroless copper line is also a major source of chelated, or

complexed, copper. Chelaters, such as EDTA, are common not only in the electroless bath itself, but also in the cleaner found at the beginning of the line. The discharge from this line often must be treated separately for this reason. Falling permit discharge limits and new formaldehyde regulations provided the impetus for the search for non-copper, formaldehyde-free alternatives.

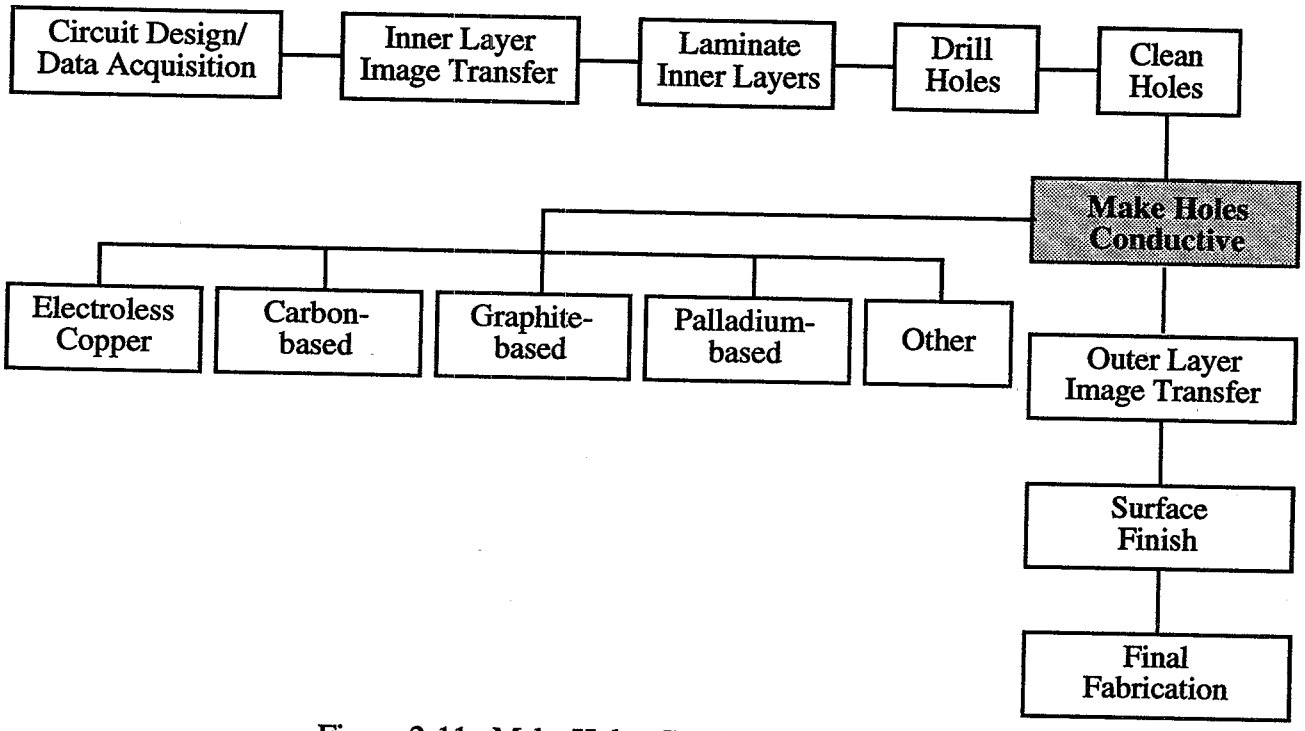

Figure 2-11. Make Holes Conductive Use Cluster.

During the first part of this decade, three basic alternatives were emerging, and still others remain to be tested. The first alternative, a carbon-based proprietary product called Blackhole®, has gained respectability and provides several definitive advantages over the conventional electroless copper process. The advantages include no chelated metal sources (in fact, aside from the conventional micro-etch chemistry, no copper sources exist at all), no formaldehyde, and a much simpler process. The same advantages are offered by the second product, a graphite-based proprietary product named Shadow®, which coats the hole barrels with conductive graphite rather than carbon. The Shadow® process contains only 4 process tanks (including a conventional micro-etch and anti-tarnish). The third alternative is a group of products that avoid the use of electroless copper by heavily seeding the holes with a palladium activator. These processes remain relatively complex (one product has nine process tanks), but are generally formaldehyde-free.

Other systems are in development. DuPont has produced an excellent technical bulletin[12] detailing 17 different approaches to direct metallization. An electroless nickel system, which has the considerable advantage of being a mature technology, is being tested, and it probably contains neither formaldehyde nor chelaters. The "Lomerson" system, described several years ago, in which the retracting drill bit smears the hole barrel with a conductive substance, continues to generate interest due to its obvious efficiencies.

12 Direct Metallization - Overview, Technical Bulletin 9410, DuPont Electronic Materials.

Despite the commercial availability of the aforementioned three alternatives, electroless copper remains entrenched as the dominant process. Many shops have waited for second or third generation products and do not feel compelled to change. Nevertheless, the industry appears poised to move away from electroless copper during the remainder of this decade.

2. Electroless Copper

The electroless copper process consists of four basic segments: cleaning, activation, acceleration, and deposition (Figure 2-12). An anti-tarnish bath is common after deposition. Virtually all shops purchase a series of proprietary chemistries from a single vendor that are used as the ingredients for the several process baths in the electroless copper process line. Only the micro-etch, its associated sulfuric dip, and the anti-tarnish baths are likely to be non-proprietary chemistries.

a. Cleaning

The cleaning segment begins with a cleaner-conditioner designed to remove organics and condition (in this case swell) the hole barrels for the subsequent uptake of catalyst, followed by a micro-etch step. The cleaner-conditioners are typically proprietary formulations, and mostly comprised of common alkaline solutions. Micro-etching, found on many PWB process lines, is itself a cluster of three chemistry alternatives: sulfuric acid-hydrogen peroxide (consisting of 5% sulfuric acid and 1% to 3% peroxide) is most common, followed by sulfuric acid-potassium (or sodium) persulfate (5% sulfuric, 8 to 16 ounces/ gallon persulfate), and ammonium persulfate. In each case, the micro-etch bath is followed by a sulfuric acid dip, which serves to remove any remaining oxidizer. The sulfuric-peroxide bath has some advantages, including high copper capacity (3 to 4 ounces/gallon) and easy waste treatment (chilling to <40°F causes copper sulfate crystallization). Ammonium persulfate is uncommon due to high waste treatment costs.

b. Activation and Acceleration

Activation, through use of a catalyst, consists of two process tanks. A pre-dip, for the drag-in protection of the expensive activation (also called catalyst) bath, usually contains hydrochloric acid and possibly tin or sodium chloride. The activation bath itself consists of hydrochloric acid, tin chloride, and palladium chloride. The Sn^{+2} ion reduces the Pd^{+2} to Pd, which is deposited on the panel. The remaining Sn^{+2} and Sn^{+4} are selectively removed from the hole barrels by the accelerator (also called the post-activator). Fluoboric acid is a common accelerator, as is sulfuric acid with hydrazine.

c. Copper Deposition

Electroless copper baths can be divided into two types: heavy deposition baths (designed to produce 75 to 125 micro-inches of copper) and light deposition baths (20 to 40 micro-inches). Light deposition must be followed immediately by electrolytic copper plating. The more common heavy deposition can survive the outer layer imaging process and copper electroplating occurs thereafter. The main constituents of the electroless copper chemistry are sodium hydroxide, formaldehyde, EDTA (or other chelater), and a copper salt. In the complex reaction, catalyzed by palladium, formaldehyde reduces the copper ion to metallic copper. Formaldehyde (which is oxidized), sodium hydroxide (which is broken down), and copper (which is deposited) must be replenished frequently.

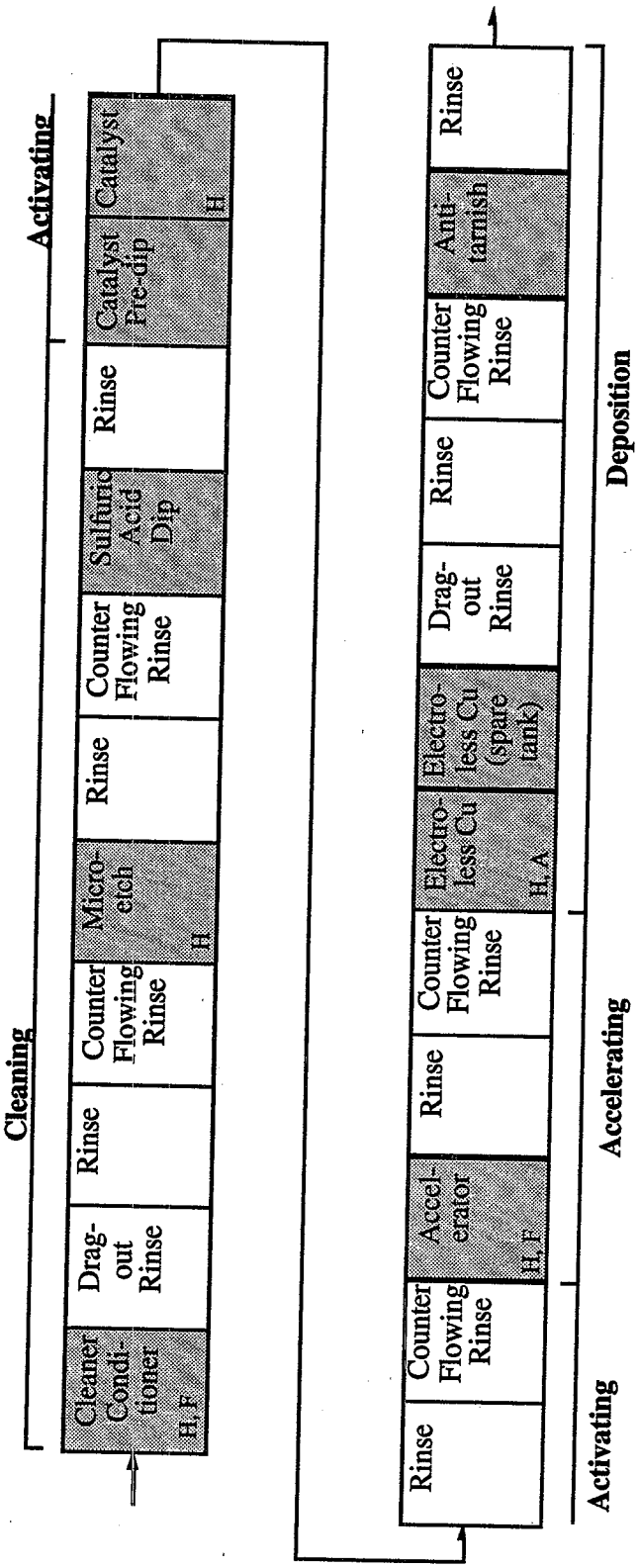

Figure 2-12. Typical Electroless Copper Plating Line.

Most heavy deposition baths have automatic replenishment schemes based on in-tank colorimeters. Light deposition formulations may be controlled by analysis. Formaldehyde is present in light deposition baths in a concentration of 3 to 5 grams/liter, and as high as 10 grams/liter in heavy deposition baths.

When light deposition is applied, the next process step must be electrolytic copper plate. This is either a full panel plate (the typical 1 mil is plated in the holes and on the surface) or a "flash" panel plate, designed only to add enough copper to the hole barrels to survive the imaging process. Flash-plated panels return to copper electroplating after imaging to be plated up to the required thickness. This double plating step has made heavy deposition the more common electroless copper process.

d. Process Waste Streams

The electroless copper line typically contributes a significant portion of a PWB shop's overall waste. Water use is high due to the critical rinsing required between nearly all of the process steps. Copper is introduced into the waste water stream due to drag-out from the cleaner-conditioner, micro-etch, sulfuric, accelerator, and deposition baths. Much of this copper is complexed with EDTA and requires special waste treatment consideration. Furthermore, waste process fluid generation is high. Micro-etch baths are exhausted when 2 to 4 ounces/gallon of copper is dissolved and this bath life is usually measured in days. While the electroless copper bath is relatively long-lived (usually several weeks or months), a considerable bail-out stream (including formaldehyde) is generated (several gallons of concentrated bath chemistry per day in production shops).

3. Carbon-based Alternatives

The only carbon-black dispersion process (Blackhole® by MacDermid) became commercially available in 1989. The advantages of this type of process versus conventional electroless plating are numerous, if one assumes that overall performance is similar (performance parity has not been established). Production rates are higher for Blackhole® since it is applied in about half the time required for electroless copper, formaldehyde is not a constituent of any of the process formulations, and copper is dragged into the wastewater stream from only the micro-etch bath. Furthermore, overall water use is reduced. Although it has become more common in larger shops, this process is still an unusual choice for small shops with sales of less than $5,000,000/year, which account for the majority of PWB facilities in the country. Capital costs for the Blackhole® conveyorized process line are much higher than for an electroless copper tank line, and represent a barrier of entry for small shops. Payback from production time savings and waste reduction are likely to be quite long for small manufacturers.

Although originally designed for either batch immersion or continuous conveyorized spray application, refinements in the carbon-black dispersion process have eliminated the immersion option. The conveyor consists of 11 chambers, 5 process baths, 4 rinses, and 2 dryers. The cleaning and conditioning processes are plumbed to share rinse water—fresh water is used for the conditioner rinse and then re-used for the cleaning rinse before being discharged from the system. The carbon-black dispersion bath itself follows. The carbon deposition layer is dried and then removed selectively from the surface copper foil by a conventional persulfate micro-etchant. A conventional anti-tarnish is the final step in the process. The anti-tarnish and micro-etch processes are also plumbed to share rinse water.

Processed panels proceed to either imaging or panel plating. No special considerations or downstream process changes are required. The carbon layer is rapidly coated with copper during electrolytic

copper panel or pattern plating and the resulting through-hole interconnection has passed industry standard performance testing (such as MIL-P-55110D).

4. Graphite-based Alternative

The only available graphite-based process (Shadow® by Electrochemicals) is very similar to the carbon-based alternative discussed above. In this case, graphite particles suspended in a colloid are dispensed onto the surface and act as conductive pathway for electroplating. The graphite solution is proprietary. Four specific process steps are required: cleaning/conditioning, graphite (Shadow®) application, micro-etch, anti-tarnish. Graphite application can be done on conveyorized equipment or with an immersion (vertical) process. One pass through the graphite application step is sufficient to prepare holes for copper deposition. The vendor claims to be able to run this process from cleaning to lamination in less than 15 minutes.[13] Graphite particles adhere well to the laminate surfaces and can tolerate mechanical scrubbing. The micro-etch solution is usually based on persulfate. Some facilities do not use anti-tarnish coatings on the copper surface if the dry film lamination process is done in-line immediately following graphite application.

a. Cleaning and Conditioning

Panels can be cleaned using conventional methods or in the conveyor line. Cleaning solutions used are similar to systems employed for electroless copper. As noted above, the cleaner-conditioner step is designed to remove organics and condition hole barrels for the subsequent uptake of catalyst or graphite in this case. Wet chemical and dry etch methods for cleaning and conditioning are discussed in Section II.E.2.

b. Graphite

The graphite is applied in the form of colloidal graphite. The particles are suspended in a slightly caustic colloidal solution (pH = 9). In the conveyorized process, up to 200 18" x 24" boards come out of the cleaning step and are dipped through a liquid colloid-containing graphite. Surface activation is rapid and solution that runs off the boards can be reused. In an immersion (vertical) setup, conventional process tanks are used to apply graphite. In this case, some efficiency is lost but existing equipment can be used. Following the graphite application, the panels must be dried to fix the graphite on dielectric surfaces. This step is critical for obtaining good copper adhesion during subsequent copper plating. Drying is done with air knives followed by a short bake (170°C). The air knives used are run at close to room temperature; their principal function is to knock excess solution off the panels. As such, these air knives consume far less energy than ones used for hot air solder leveling (HASL). Very little waste is generated during graphite deposition because panels are dipped through a graphite-containing solution. No rinse is required.

c. Micro-etch

Micro-etch follows graphite application. The drying step does a good job at removing colloid material from the field area of the panel. However, simply drying the solution does not remove graphite particles from exposed copper. The vendor recommends spraying a persulfate solu-

13 P. Goldman, "The Economics of Replacing Electroless Copper," *Circuitree*, February 1994.

tion onto the panel surface. A filter below the panels prevents graphite from entering waste streams. Also, the graphite captured at the micro-etch step is returned to the process at the graphite step.

d. Anti-tarnish

Following micro-etch, the exposed copper is subject to oxidation. Because of this, an optional "anti-tarnish" step can be done. The system vendor recommends using a benzothiadzole-containing solution to protect copper surfaces. Some PWB manufacturers skip this step, in which case it is recommended that image transfer films be laminated onto the panels directly following micro-etch. Skipping the anti-tarnish step should reduce chemical use, cost, waste, and cycle time. Effects on reliability were not reported but some commercial vendors use this approach.[14]

e. Process Waste Streams

The quantity of waste water produced by a typical horizontal conveyorized graphite application system is less than 5 gallons/minute. Also, wastewater is only produced when the system is running, rather than constantly, as in the rinse tanks used for electroless copper plating. In short, the graphite system seems to reduce both waste streams from PWB manufacturing and PWB manufacturing costs. There are five principal environmental benefits from using the graphite process instead of electroless copper. These include:

- Reduction in chelated copper and metal waste,
- Elimination of formaldehyde,
- Reduced water use,
- Reduced treatment chemical use, and
- Reduced sludge disposal.

5. Palladium-based Alternatives

Another alternative to electroless copper is palladium-based, which has the benefits of completely removing formaldehyde from the process, reducing the amount of water consumed to make drilled holes conductive, and reducing the amount of wastewater generated from such a process. It can also be run with conveyor equipment to increase throughput and lower cost. Like the graphite process discussed above, panels can be sent directly from a palladium-based process to a dry film laminator.

a. Cleaner/Conditioner

The first stage of cleaning/conditioning is the "sensitizer" step. Two things must be accomplished: first, through-holes must be cleaned, and second, a charged polymeric material must be applied to the inside dielectric surface of holes. This charged material can then receive a catalyst during subsequent processing. Cleaning is accomplished with the desmear chemicals discussed in Section II.E.2. Chemical use and waste water produced in the cleaning step of the palladium-based process is similar to volumes used for the carbon- and graphite-based processes. However, each step must be followed by a rigorous rinse to prevent contamination of the following steps.

14 Direct Metallization - Overview, Technical Bulletin 9410, DuPont Electronic Materials.

- Pre-dip: During pre-dip, a base salt version of the catalyst (which does not contain catalyst metal) is applied to the panels.
- Activator: After pre-dip, the catalyst (activator) is applied. In this case the catalyst is palladium/ tin in a colloidal solution. The catalyst adheres well to glass/epoxy laminates.
- Accelerator (Enhancement): After the activator step, panels are rinsed with a caustic soda (accelerator or enhancer). The accelerator removes stannous tin (Sn^{+2}) or reduces it to a metallic form (Sn). Also during this step, metallic palladium is converted to palladium sulfide (PdS).
- Stabilization
- Alkaline Rinse

b. Micro-etch

Micro-etch is done with hydrogen peroxide (H_2O_2) and sulfuric acid (H_2SO_4). This step removes excess palladium sulfide from exposed copper surfaces without oxidizing the copper. This step enhances adhesion between exposed copper and electroplated copper added later without degrading adhesion between laminate materials and plated copper.

c. Drying

After micro-etch, the panels are dried to prepare them for lamination.

d. Process Waste Streams

There are two principal process waste stream considerations: first, formaldehyde is completely eliminated from the process of making holes conductive; and second, the amount of water used (and waste water produced) is greatly reduced when compared to conventional electroless plating. According to Shipley, the maker of one palladium-based process, the cost of this process is competitive with electroless copper plating.

G. Outer Layer Image Transfer

1. Overview

This large cluster includes outer layer imaging, copper plating, etch-resist plating or application, etching, and etch-resist stripping (Figure 2-13). The cluster includes copper electroplating, a function not normally associated with image-transfer copper-plating. Although arguably an independent function, copper electroplating is performed in a sequence determined by the overall image transfer strategy. Furthermore, with copper sulfate being the overwhelming choice of PWB shops, a cluster of alternatives does not actually exist (pyrophosphate baths, the other chemistry, have vanished). With the exception of process material improvements such as dry film photoresist, plating chemistries (copper sulfate vs. pyrophosphate, in particular), or the substitution of tin-only etch-resist for tin-lead, this cluster has remained essentially unchanged for many years. It also forms the core of double- and single-sided processing, thus many of the processes described here predate multilayer manufacturing.

Two major subtractive options, starting with copper clad laminant, are available to the PWB manufacturer. The first sequence, print, pattern-plate, and etch, is the most common. While copper pattern-plating is a uniform process shop-to-shop, the etch-resist metal plated over the copper is not and

forms an interesting and important second level cluster. Etching is theoretically a cluster of two chemistry options, but with most metallic etch-resists, only ammoniacal is possible. In the other sequence, panel plate, print, and etch is less common. Here, copper is plated to full thickness over the entire panel prior to imaging. The photoresist imaged during the "print" process serves as the etch-resist precisely as in inner layer image transfer.

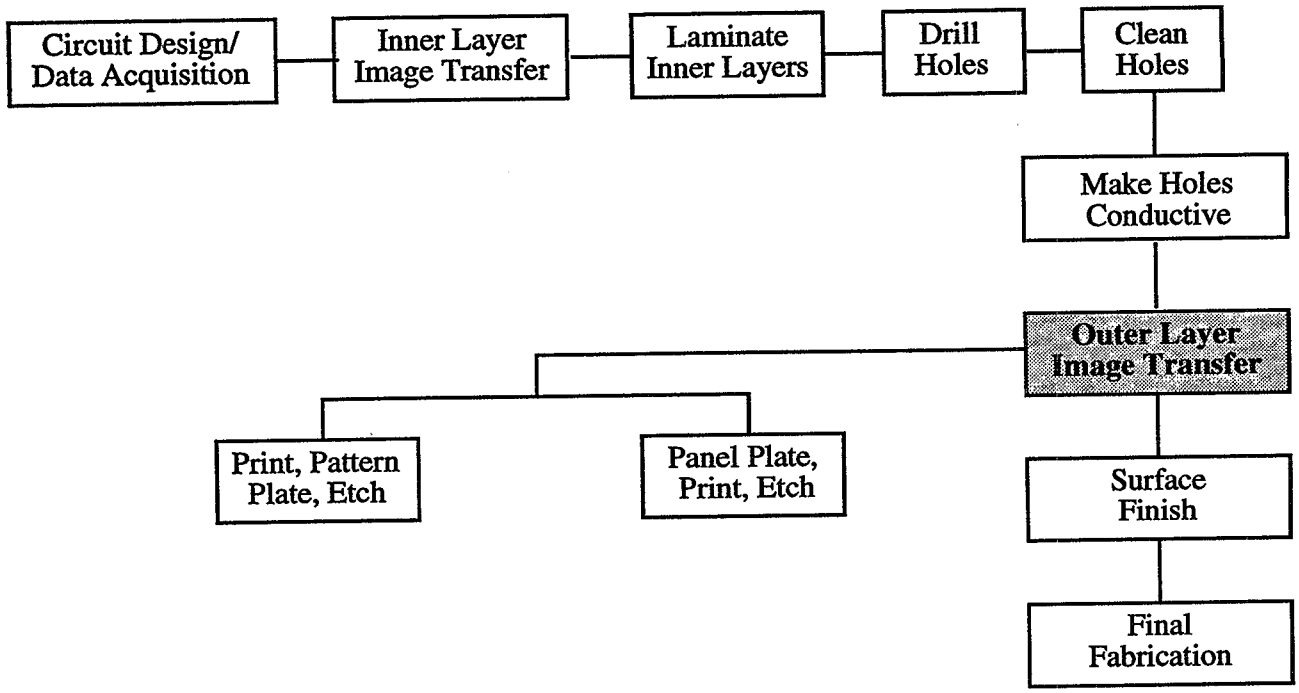

Figure 2-13. Outer Layer Image Transfer Use Cluster.

It can be seen that the panel plate, print, and etch process (also referred to as "tent-and-etch" because the drilled holes are tented over and protected from the etchant by dry-film photoresist) eliminates process steps required in the more common pattern-plate process. There is no etch-resist plating (the photoresist serves as the etch-resist) or metal stripping Therefore, the tin or tin-lead problem is obviated. Furthermore, cupric chloride etching is an option when dry-film photoresist is the etch-resist. Unfortunately, it is the inefficiency of panel plating, along with certain technical limitations of this process, that prevent its widespread use. Most of the copper on a typical circuit panel is etched away, thus most of the plated-on copper of this process is promptly removed during etching, unlike the copper added during pattern plating. Furthermore, the panel-plated copper can cause difficulty in etching, particularly fine-line etching. The thicker the copper to be etched, the greater the undercut. This problem has dampened the enthusiasm for tent-and-etch. On the other hand, layout design changes can easily rehabilitate tent-and-etch. One method, referred to as "pads-only outer layers" eliminates difficulty of fine-line etching on outer layers (along with eliminating the need for solder mask) at the expense of requiring two extra layers of inner layer circuitry.

It should be pointed out that several of the process options listed here and in Section II.H are not true options, but rather, alternative methods required in some cases by customer specification and end-product performance. Although tin and tin-lead perform identically as etch-resists, shops that are otherwise anxious to remove lead plating are unable to do so. A small number of parts continue to require reflow (a finish necessitating tin-lead plating) rather than hot-air-solder-level (HASL) (a finish for which tin can be substituted for tin-lead).

2. Image, Pattern Plate, and Etch

a. Imaging

Outer layer imaging is quite similar to inner layer imaging. The panel is thicker and has drilled holes, but it is essentially processed the same. Small shops may use the identical photoresist product for both inner and outer layers for convenience. Photoresist thickness, not critical for an etch-resist, takes on significance as a plating resist. Most shops use a thinner resist for inner layers (0.001 inches) and are forced to use thicker resist for outer layers (typically 0.0015 or 0.002 inches). Generally, the resist thickness should equal or exceed the thickness of the metals to be plated onto the pattern to avoid copper or tin-lead "mushrooming" over the top of the resist. Resists other than dry film are extremely uncommon for outer layer imaging.

Exposing may be done with first-generation photo-plotted photo-tools or with diazo, a reddish transparent film that allows for manual registration. With a diazo photo-tool, an operator can see through the dark areas of the film (the circuit pattern) and can align the photo-tool to the hole pattern, eliminating the need for tooling regimes. Although not practical for production shops, manual registration with diazo photo-tools is not uncommon in prototype shops. When pattern plating is to follow, outer layer photo-tools are positive images of the circuit. When developed, the circuit image is developed away, exposing the underlying copper. The photoresist remaining on the panel is the plating resist for the pattern plate process. Developing is done in a sodium carbonate solution (1% to 2%).

b. Pattern Plating Copper

Pattern plating, so named because only the circuit pattern and hole barrels are plated, is a two-step process (Figure 2-14). First, copper is plated. Only the thin electroless copper layer has been deposited in the hole barrels up to this point in the process and it is far short of the typical 0.001-inch specification for copper thickness. Copper is also plated onto the circuit pattern. None of the copper plated during this process is etched away, but rather, remains on the circuit and is part of the finished product. Second, immediately after copper electroplating, a metallic etch-resist is plated over the copper, usually tin, tin-lead or nickel-gold.

Although a few copper electroplating chemistries exist, nearly all modern PWB shops use simple copper sulfate. The bath has an extremely long life (measured in years) and is generally easy to maintain and control. The bath is typically made with 10 ounces/gallon of copper sulfate, 25 to 40 ounces/gallon of sulfuric acid, and a small amount of hydrochloric acid to provide a chloride concentration of 30 to 90 ppm. Proprietary organic additives, usually referred to as brighteners, distinguish one vendor's bath from another. The pre-plate line consists of an acid cleaner (dilute phosphoric acid is a common constituent), a micro-etch, and a sulfuric pre-dip.

High-performance copper plating is reliably performed at a current density range of 20 to 35 amperes/ft^2. Manufacturers generally plate from 0.0013 to 0.0017 inches of copper to ensure that all hole barrels meet the minimum of 0.001 inches in all areas of the panel. Dwell times depend on current density and target thickness, but generally range from 30 minutes to somewhat more than one hour. Although a source of copper in the waste water stream, the copper sulfate plating process lends itself to several recovery schemes. A drag-out tank immediately following the plating bath can be electrowinned (an electrolytic recovery process) while in service to maintain a low copper concentration therein (reducing copper dragout to the flowing rinses), while recovering dragged-out copper in metallic form. Some have employed ion exchange to produce a closed-loop. In this arrangement, waste water is purified and reused as rinse water and the cation regenerant is returned to the copper sulfate bath.

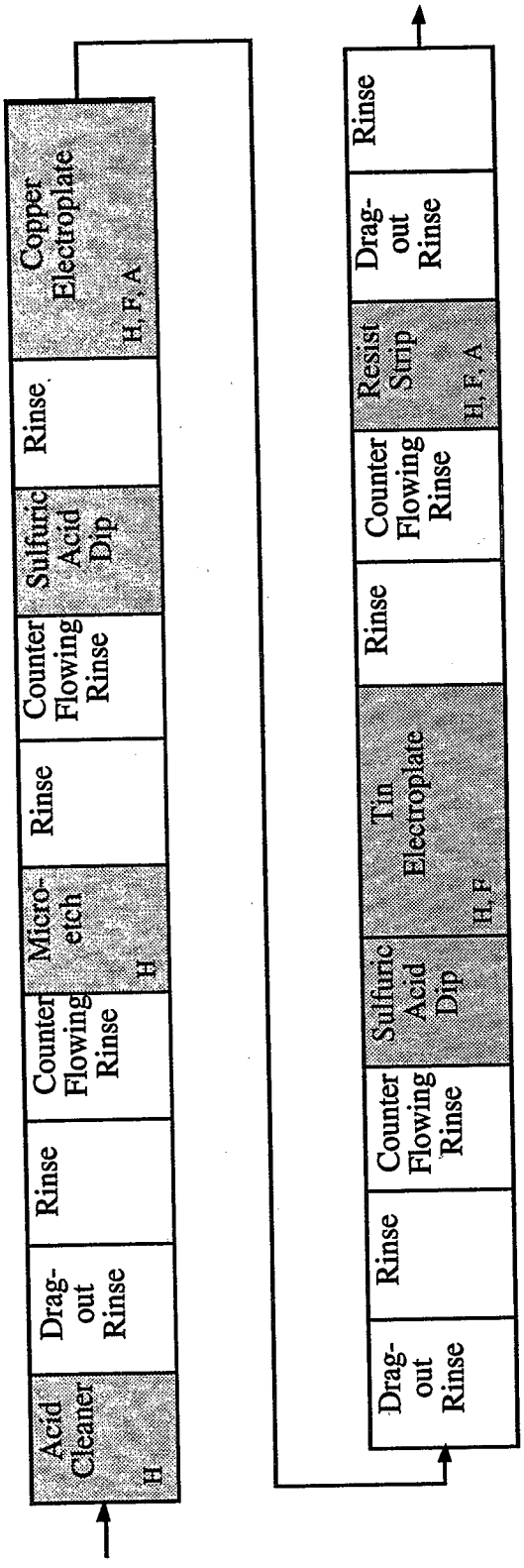

Figure 2-14. Typical Pattern Plate, Etch-Resist, Photoresist Strip Process Line.

c. Pattern Plating Etch-Resist

Immediately after copper pattern plating, an etch-resist metal is plated over the copper. Tin-lead has been the most common etch-resist for the simple reason that in cases where the surface finish is reflowed solder, tin-lead efficiently serves as both etch-resist and finish. With the rise of the solder-mask-over-bare-copper (SMOBC) surface finish method, tin-lead plating has become unnecessary for most panels. Shops facing prohibitive lead discharge limits have rapidly embraced tin-only plating, which has become the primary alternative. While the regulatory status of tin varies from locality to locality, it is safe to say that tin concentration receives considerably less scrutiny than lead. Many shops have, however, been reluctant to eliminate tin-lead plating due to the fact that a certain percentage of their work still requires a reflowed finish. Some military specifications continue to call for tin-lead reflow so tin-lead plating is quite common in shops serving military clients. Still other shops have been forced to maintain both tin and tin-lead plating baths to satisfy their customer base. As an etch-resist, there is no difference in the performance of tin or tin-lead.

Two tin-lead plating chemistries currently exist. The fluoborate bath is most common. This bath consists of fluoboric acid, tin and lead fluoborate, and proprietary organic additives. Stannous tin (Sn^{+2}) is maintained at 2 to 4 ounces/gallon and lead at 1 to 2 ounces/gallon. The other chemistry, which is entirely proprietary, consists of methane sulfonic acid (MSA) and is not in wide use. Tin-lead is plated to a thickness of 0.0002 to 0.0005 inches.

Tin fluoborate can be used as an alternative to tin-lead plating. Some shops have phased out tin-lead by simply replacing the tin-lead anodes in the fluoborate bath with tin anodes, allowing the lead concentration to gradually fall. Tin sulfate, however, has become the tin bath of choice. Tin is plated for etch-resist purposes only—a 0.0002 inch thickness is adequate. The sulfate bath consists of 20% sulfuric acid and enough stannous sulfate to provide 2 to 3 ounces/gallon of stannous tin.

Nickel-gold is also pattern plated electrolytically as an etch-resist and surface finish. Electrolytic soft gold is the surface finish of choice for certain performance considerations, including high corrosion resistance, low contact resistance (although wear resistance is poor), and long shelf-life. Electrolytic pure gold may be called for on circuits requiring wire bonding. The nickel-gold plating line consists of a nickel pre-dip, the nickel plating bath, a gold pre-dip, and the gold plating bath. The nickel plating chemistry of choice is nickel sulfamate or nickel sulfate. Nickel is quite concentrated in either bath and reaches 17 ounces/gallon in typical nickel sulfate formulations. Unlike many other process baths, many shops use decades-old nickel plating formulations and do not purchase proprietary chemicals. Nickel is plated to any specified thickness, usually in the range of 50 to 500 micro-inches. Gold is then immediately plated over the nickel. Acid gold cyanide formulations are most common and are similar, but not identical, to the hard gold baths designed for edge connector plating. Sulfite-based alkaline baths are also in use. Gold is generally plated to a thickness under 100 micro-inches, and for many applications 10 to 30 micro-inches will suffice. Both the nickel and gold plating baths are quite long-lived—barring unusual events, each may be maintained for several years.

Other etch-resists include tin-nickel and tin-lead over tin-nickel, well-known to have certain performance advantages over conventionally processed boards, but are rarely found. Metals such as rhodium or gold may be plated selectively over certain areas of a circuit, then masked off and a conventional etch-resist is plated over the remainder. Rhodium is the metal of choice for maximum wear resistance.

d. Photoresist Stripping

Photoresist is stripped from the outer layers in the same chemistry (often in the same bath or spray chamber) as the inner layers. When tin-lead is the etch-resist, small amounts of lead can be removed as metal or dissolved in the stripper solution, which complicates waste treatment. It should be noted that, although resist stripping is a simple, one-tank operation, the majority of a shop's total resist consumption is dissolved in this bath (the remainder is dissolved in the developer). Both the developer and the stripper have very short bath lives (often measured in hours) compared to most plating solutions, and these operations generate a large volume of waste process fluid.

e. Outer Layer Etching

Ammoniacal etchant is the only etchant used for outer layer panels plated with a metallic etch-resist (Figure 2-15). The etchant is generally inert to both tin and lead, although some manufacturers do report low concentrations of lead present in their spent ammoniacal etchant. Etching of outer layers is otherwise identical to that of inner layers described in Section II.B.2.e. Spent ammoniacal etchant is a major waste stream and is usually transported to recycling plants.

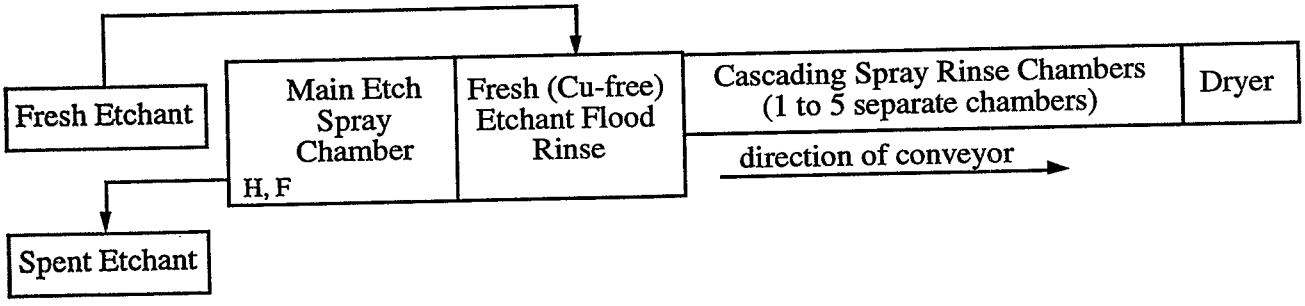

Figure 2-15. Typical Ammoniacal Etch Process.

f. Tin and Tin-Lead Stripping

Etch-resist is stripped off the panel immediately after etching for the solder mask on bare copper (SMOBC) process. Tin-lead may remain on the board if reflowed tin-lead is the specified finish; in these cases the strip process is bypassed. Previously, reflow was a common finish. It is now quite rare for multilayer circuits, but still is found in "low" technology single- and double-sided circuits. Tin or tin-lead stripping chemistry is proprietary. Nitric acid, ammonium bifluoride, and peroxide-based systems are available. The stripper bath-life is moderate. If lead is present on the surface, the spent process fluid from this bath is the major source of waste lead.

3. Panel-Plate, Print, and Etch ("Tent-and-Etch")

With the exception of the additional panel plating (so named because the entire panel is plated, not just the circuit image) step, this process precisely tracks the inner layer print-and-etch method described in Section II.B.2. Outer layer image transfer is accomplished in fewer process steps, requires less time, and creates somewhat less waste. Although copper is inefficiently plated, then etched, etching can be performed in cupric chloride or ammoniacal systems.

One major drawback of tent-and-etch is the difficulty of etching through the plated-on and base-laminate copper layers. With circuit densities steadily increasing, circuit features have become smaller and smaller. Most shops are required to produce patterns of trace widths that measure less than 10 mils across. Fine-line etching is quite difficult if the sum of the copper residing on a panel is 2 to 3 mils thick, which is the typical sum of 0.5 ounce/ft^2 base laminate copper and the panel plating. A second problem arises when SMOBC is not the surface finish required. Electrolytic gold and tin-lead must be pattern plated in most cases. Thus, a shop faced with a variety of requirements cannot use tent-and-etch exclusively.

H. Surface Finish

1. Overview

For most parts, the functions of the surface finish are to prevent copper oxidation, facilitate solderability, and prevent defects during the assembly process. Other surface finishes are dictated by the environment in which the part will reside or by specific performance criteria. It is in outer layer finishing that the greatest variety of manufacturing options and processes exist (Figure 2-16). Furthermore, the exact sequence of the processes in this cluster may vary from shop to shop. For example, gold edge-connector plating may occur either before or after solder mask application.

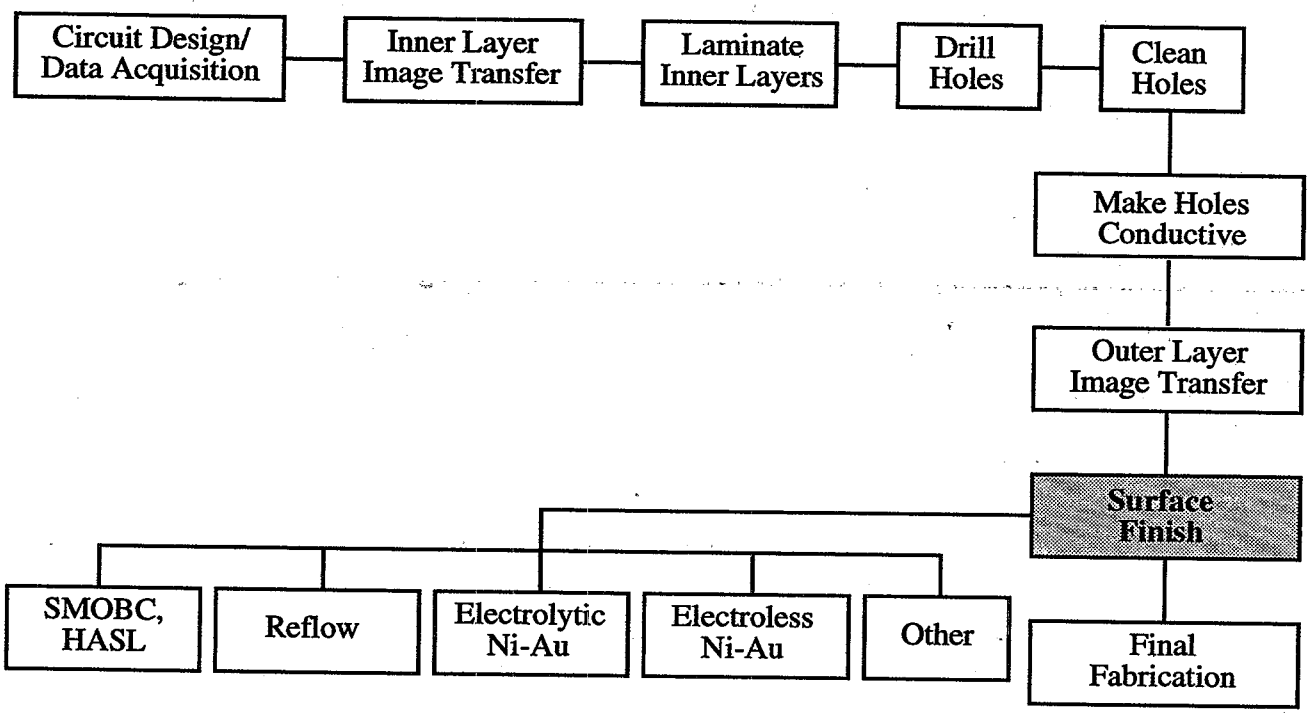

Figure 2-16. Surface Finish Use Cluster.

Solder-mask-over-bare-copper (SMOBC) with hot-air-solder-leveling (HASL) has become the industry-wide standard finish, replacing tin-lead reflow, which is now an unusual finish for multilayer parts. Nickel-gold is a significant alternative finish. Nickel-gold coatings may be electrolytically plated as an etch-resist (a direct substitute for tin or tin-lead) or they may be applied electrolessly after solder mask application (a direct substitute for HASL). Organic, "pre-flux" coatings, which prevent oxidation and facilitate subsequent soldering, are gaining in popularity. Beyond these finishes are a wide variety

of combinations that vary from shop to shop—selectively plated combinations of gold, tin-lead, and even rhodium. Shops have produced SMOBC, tin-lead reflow panels by plating tin-lead as an etch-resist, then after etching, selectively stripping it in all area except pads and hole barrels. After solder masking, the panels are reflowed.

2. Solder Mask Over Bare Copper (SMOBC), Hot Air Solder Level (HASL)

This method predominates for several reasons. Copper is a surface that lends itself to rigorous cleaning, which is essential for solder mask adhesion. Tin-lead under solder mask will liquefy during soldering and may cause the mask to blister and peel. The hot air solder leveling process generally produces less waste water and introduces less lead into the waste water stream than tin-lead plating and reflow. Despite these advantages, well-known disadvantages also exist. The shelf-life of hot air solder leveled circuits is short and solder thicknesses on pads and hole barrels is notoriously difficult to control. For these reasons, a small minority of specifications continue to call for tin-lead plate and reflow or other alternatives. The overall process consists of a solder-mask pre-clean, usually a mechanical or pumice scrub. Solder mask is then applied, followed by hot air solder leveling, nomenclature screening, and finally, gold edge plating if necessary.

a. Solder Mask

The purpose of solder mask is to mask off and insulate physically and electrically those portions of the circuit to which no solder or soldering is required. Increasing density and surface mount technology have increased the need for solder mask to the point that, with the exception of "pads only" designs, nearly all parts require it. Manufacturers have had some autonomy in selecting masks. Many specifications do not call out a specific product or product type and this has allowed the manufacturer to choose masks based on processing as well as performance issues.

Three basic type of masks are commonly applied: thermally cured screen printed masks, dry film, and liquid photoimagible (LPI). Thermal masks have predominated for decades but are gradually being replaced by LPI, despite being the lowest cost alternative. Dry film has some specific advantages, such as ease of application, but its use seems poised to decline as well in the face of improving LPI formulations.

b. Hot Air Solder Level (HASL)

The HASL process consists of a pre-clean, fluxing, hot air leveling, and a post-clean. Pre-cleaning is usually done with a micro-etch. However, the usual persulfate or peroxide micro-etch is not common in the process. Dilute ferric chloride or a hydrochloric-based chemistry is favored for compatibility with the fluxes that are applied in the next step.

Hot air level machines consist of a panel transport mechanism that carries the panel into a reservoir of molten solder, then rapidly past jets of hot air. All areas of exposed copper are coated with solder and masked areas remain solder-free. Boards are then cleaned in hot water, the only step in the SMOBC process where lead may enter the waste water stream, albeit in very small quantities. Once cleaned, the panels may again enter the screening area for optional nomenclature screening, or proceed directly to the routing process.

3. Reflowed Tin-Lead

The reflow process, once the predominate method, uses the tin-lead etch-resist to create the final surface finish, thereby creating some efficiency when compared to the plate-etch-strip sequence of SMOBC. It is not uncommon in lower-technology designs. Some military specifications require reflow and explicitly exclude the SMOBC/HASL method. Tin-lead is required, however, and this has contributed some to the demise of reflow. Distinct performance issues have also played a role—tin-lead is difficult to clean, is a poor surface for solder mask, and will liquefy during wave soldering, causing defects downstream. The basic function of the reflow process step is to fully encapsulate the copper on the panel (after etching, copper is exposed along the vertical flanks of circuit features) and to create a more durable surface.

Two types of reflowing, or fusing, methods exist. The oldest is hot oil reflow. In this process, the board is fluxed, then immersed in a pot of hot oil long enough to heat the tin-lead plate to its melting point. Infra-red reflow, a somewhat more modern approach, is done in a conveyorized machine that includes a fluxing station, an infra-red oven chamber, and a cool-down chamber.

4. Nickel/Gold

Nickel-gold finishes may cover an entire circuit or be selectively plated onto certain areas of a circuit. Furthermore, nickel-gold formulations produce hard (cobalt or other metal is co-deposited in small amounts for hardness) or soft deposits (pure gold). And, nickel-gold can be either electrolytically or electrolessly deposited.

a. Hard Gold

Hard gold is electrolytically plated. The most common application of hard gold is edge connectors, but hard gold may also be plated over circuit areas as well. Automated edge plating machines are common since manual plating is quite labor-intensive. Typically, a plater's tape is applied to the board, masking off all of the circuit above the edge connector area. The panel is then processed through a nickel-gold plating line, with just the edge connectors immersed in the plating fluid. Nickel is plated first and Watts or sulfamate nickel is common. Cyanide gold is the most common gold electroplating chemistry.

b. Soft Electrolytic Gold

Soft gold is a pure gold over nickel deposit. It may be plated over the entire circuit or selectively over certain portions of a circuit (excluding edge connectors, which require hard gold). Selective electroplating requires a combination of masking and bussing (providing current to the portion of the circuit being electroplated). Selective gold applications include contact points (which may require hard gold), press pads, wire bond sites, or portions of a board that may reside in a corrosive environment. Selective gold plating can be labor-intensive and is not frequently specified for production lots (all gold plating is often substituted; the labor savings offset the extra gold).

c. Electroless Nickel/Immersion Gold

This method of applying soft gold has received considerable attention. Electroless plating can be conveniently performed after etching because no bussing is required. Therefore,

these all-gold boards can be processed with a standard tin etch-resist and processed identically as SMOBC, except the gold plating step replaces the HASL step. This process has advantages over SMOBC/HASL and electrolytic gold plating. When compared to SMOBC/HASL, electroless all-gold circuits have a much longer shelf life. The flat surface profile of the electrolessly plated surface-mount pad and overall excellent solderability make electroless nickel/gold ideal for surface-mount technology. When compared to electrolytic gold, electroless has the advantage of full copper encapsulation because plating is performed after etching, not before, as with electrolytic gold plating. Selective gold plating is made somewhat easier by the electroless plating method since no electrical bussing is required. Cost is the main disadvantage. Immersion gold and electroless nickel process baths are short-lived compared to electrolytic formulations and maintenance and control of these baths is more difficult. The main application of electroless nickel-gold coatings is chip-on-board technology, where component leads are ultrasonically or thermosonically bonded to gold pads rather than soldered.

I. Final Fabrication

During the final fabrication process, non-plated through-holes and other tooling features may be added to the circuit, and the circuit itself is completely or partially depanelized. Depanelization is accomplished with numeric controlled routers that are quite similar to drilling machines. With complete depanelization, the circuit is routed out of the panel. With partial depanelization, common with production lots, most of the circuit profile is routed, but it remains tabbed to the panel during testing and assembly. In this way , several circuits can be tested and assembled at once. After assembly, the individual circuits of a panel can be conveniently snapped, or broken, out of the panel. Such panels are often referred to as "breakaways" or "snaps." Tool-and-die depanelization methods are not common with multilayer circuits.

III. SUPPORT OPERATIONS

A. Waste Treatment

Because of their toxicity, certain cations are of great importance in the treatment and disposal of waste water. Copper, lead, silver, tin, and chromium are toxic in varying degrees to microorganisms used in publicly-owned waste treatment facilities and therefore must be taken into consideration in the disposal of PWB effluents. Some publicly-owned waste treatment facilities have been upset by the introduction of these ions, because microorganisms were killed and their ability to clean water ceased. In sludge digesters, copper is toxic at a concentration of 100 milligrams/liter, chromium and nickel are toxic at concentrations of 500 milligrams/liter, and sodium is also toxic at high concentrations. Other toxic cations include potassium and ammonium at 4000 milligrams/liter. Some toxic anions, including cyanides and chromates, are also present in PWB waste streams. These are found particularly in metal-plating effluents.[15]

Treatment of waste streams at the manufacturing site requires capital investment, but it is required by governmental regulations. Federal statutes of this type include the Clean Water Act (CWA) and the Resource Conservation and Recovery Act (RCRA). Over the last 30 years, the number of federal laws regulating environmental issues has gone from less than 10 to more than 40.[16] A proactive policy of waste reduction will help make the industry robust to variations in the regulatory environment.

B. Waste Streams

1. Solvents

Solvents are used to strip dry-film laminates and for other cleaning applications. Monoethanolamine is often the chemistry of choice for removing dry-film laminates. Other proprietary formulations exist as well. Methylene chloride was formally used for stripping negative working resist materials; however, it is declining in use, and is unnecessary for fully aqueous films. Alcohol and acetone are often used for simple cleaning operations.

2. Process Baths

Electroless copper lines contribute a large portion of the overall waste from PWB manufacturing. Water use is high due to the critical rinsing required between nearly all of the process steps. Rinse water waste from electroless copper lines is problematic in several ways. Copper is introduced into the waste water stream due to drag-out from the cleaner-conditioner, micro-etch, sulfuric, accelerator, and deposition baths. This copper is usually complexed with EDTA and requires special waste treatment consideration. The volume of waste generation is high, but the concentration of valuable material to recover is low. Since the waste generated does not have very high value as a reclamation material, rewards for regeneration are relatively low. Micro-etch baths are exhausted when 2 to 4 ounces/gallon of copper is dissolved, and this bath life is usually measured in days. While the electroless copper bath is relatively long-lived (usually several weeks or months), a considerable bail-out stream is generated (several gallons of concentrated bath chemistry per day in production shops).

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15 Metcalf and Eddy, Wastewater Engineering: Treatment, Disposal, Reuse, 2nd Ed., McGraw-Hill series in water resources and environmental engineering, 1979, p. 102-104.

16 G. Pitts, R. Ferrone, et al., "Environmental Consciousness: A Strategic Competitiveness Issue for the Electronics and Computer Industry (Summary Report)," an Industry-led Study Sponsored in part by The U.S. Department of Energy and coordinated by The Microelectronics and Computer Technology Corporation (MCC), March 1993, p. 2.

In addition to waste water, the electroless copper plating process also generates significant volumes of formaldehyde, which is one of the most hazardous chemicals used in PWB manufacturing (formaldehyde is very volatile and requires sufficient ventilation to minimize worker exposure). Concentrations of 3 to 10 grams/liter are common in electroless plating baths. Formaldehyde enters the waste stream through drag-out from electroless plating, and it is oxidized in the plating process and must be replenished with new additions. By switching to a process (such as carbon or graphite alternatives) that does not use electroless copper plating to make holes conductive, two important environmental benefits can be obtained: first, formaldehyde is completely eliminated from the process of making holes conductive, and second, the water used (and waste water produced) is greatly reduced when compared to conventional electroless plating.

IV. SELECTING A USE-CLUSTER FOR A DfE PROJECT

A. Cleaner Technologies Substitutes Assessment

In a DfE pwb project, a use cluster is selected to become the focus of a Cleaner Technologies Substitutes Assessment (CTSA). The CTSA is a flexible format for systematically comparing trade-off issues associated with traditional and alternative chemicals, processes, and technologies. For each chemical, process, or technology, the cost, performance, environmental and health risks, environmental releases, energy impacts, and resource conservation implications are evaluated. The goal of the CTSA is to allow for an informed decision about which alternative is best for a particular situation.

B. Use Cluster Scoring System

EPA's Office of Pollution Prevention and Toxics (OPPT) has developed a system for use in screening and prioritizing use clusters, referred to as the Use Cluster Scoring System (UCSS). The UCSS was designed around the concept of identifying and analyzing clusters of chemicals that can be used to perform a particular task, such as those described in this report. By screening and scoring these "use clusters," efforts may be more directly focused upon effective risk reduction through work with targeted industries or users. The UCSS also assists other public and private sector organizations to identify clusters of potential concern and provide an initial ranking of chemicals using hazard and exposure data from various sources.

Data is first collected for each chemical within a cluster for a number of factors that indicate the potential for human and environmental exposure, potential for human and environmental hazard, pollution prevention potential, and EPA/stakeholder interest. This information is then entered in the UCSS using the data entry menu options.

Health and environmental risk or toxicity rating scores are calculated for each chemical within a cluster using the information entered and pre-programmed scoring algorithms. The individual chemical scores are then used to calculate an overall cluster score, which is an indicator of potential risk and pollution prevention potential for the use cluster. OPPT uses this risk score to prioritize clusters to be investigated in more detail.

C. Use Cluster Selection in the DfE PWB Project

At the beginning of the DfE PWB Project, four use clusters were defined by industry stakeholders as being of high priority for evaluation in a CTSA. The four use clusters were:

1. Inner layer etching
2. Outer layer etching and plating
3. Making holes conductive
4. Hot air solder leveling

These four use clusters were evaluated by EPA for their potential environmental risk and pollution prevention potential using the UCSS. The lowest possible score (least risk) is 4 and the highest possible score (greatest risk) is 24. The scores for each use cluster were:

1. Inner layer etching 12.3
2. Outer layer etching and plating 12.7
3. Making holes conductive 11.2
4. Hot air solder leveling 12.1

It was determined that there is no statistical difference between these scores; all fall in the "medium" range. That is, they have the potential to pose moderate risk to both humans and the environment. Use cluster scores are one of several criteria that are considered in the selection of a use cluster. The similarity in the scores, however, led to an increased emphasis on other criteria in making the selection for the PWB Project.

Because the objective of the CTSA is to evaluate alternatives, it is very important to select a use cluster with several viable alternatives. Other criteria, such as occupational health risk, industry interest, and regulatory cost/burden, should also be considered.

The first use cluster selected for evaluation in the DfE PWB Project was *making holes conductive*. Ten alternatives, the greatest number found for any of the potential use clusters, were identified for this cluster during the information gathering phase of the project. Also, the project participants believed that there were a number of relatively easily addressed environmental issues associated with the making holes conductive use cluster. Another reason that making holes conductive is a good initial use cluster for a CTSA is that some of the alternatives promise production rate benefits. The processes could be conveyerized, the production cycles could be decreased, the pre-treatment rinses could be simplified, and waste production could be reduced. In addition, simple pollution prevention practices could be implemented in the baths. While information is being gathered about new and emerging technologies, some of the current processes are undergoing revision and enhancements. The CTSA is a convenient place to assess these enhancements.

D. Future Design for the Environment Projects

This profile document has already served its original purpose in assisting the Design for the Environment PWB Project to select the first use cluster for further analysis in a CTSA. It is anticipated that the profile document will be useful in future Design for the Environment Project activities and to other interested parties wishing to use this information for their own analyses.

REFERENCES

The following is a general list of references used in the preparation of this text, but not specifically cited in the body of the report.

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Pitts, Greg, et al., "Environmental Consciousness: A Strategic Competitiveness Issue for the Electronics and Computer Industry," MCC, et al., March, 1993.

Rivera, Carlos, and Declue, Gary, "Ammoniacal Etchant Regeneration and Copper Recovery," *7th Annual AESF/EPA Conference on Environmental Control for the Surface Finishing Industry*, 1986.

U.S. EPA, "Emissions From PWB Manufacturing, Draft Report," Scientific Consulting Group, Inc., March, 1995.

Electroless Plating: Plating that proceeds without an external electricity source. A reduction of metal ions is accomplished with a chemical reducing agent (such as formaldehyde in electroless copper).

Electrowinning: A common metal recovery technology. Essentially electroplating, electrowinning is employed to electrolytically recover metal from wastewater through electrolysis. Large cathodes, and other design strategies are employed to win metal ions from dilute waste streams. Metal is recovered on cathodes for reuse or sold as scrap. The most common application is on drag-out tanks, where the fluid is continuously recycled through the electrowinner and a low concentration of metal is maintained (rather than the steadily rising concentration that would otherwise occur in a still rinse).

Etchback: A process by which an amount of printed wiring board substrate material (glass and epoxy, but not copper) is dissolved or otherwise removed from the walls of drilled holes. The purpose of etchback is to expose a greater inner layer copper surface area for interconnection with subsequently plated copper.

Etchant: In printed wiring board manufacture, a chemical that oxidizes metallic copper. Etchants are used to remove relatively thick layers (0.7 to 2.8 or more mils) of copper.

Etch-resist: A substance unaffected by an etchant that is selectively applied over copper to protect the copper from the etchant. After etching, only the copper under the etch-resist remains on the board. Etch-resists may be organic (photoresists) or metallic (tin, tin-lead, nickel-gold).

FR-4: A designation for a flame retardant that contains bromide.

Image Transfer: The series of processes by which an image of a circuit layer is transferred from film, glass, or data files to a copper layer of a printed wiring board. Image transfer is accomplished differently for both inner and outer layers. For inner layers, print-and-etch is most common, while for outer layers, print-pattern plate-etch is typical. Other methods exist.

Immersion Plating: Similar to electroless plating except that the reduction of metal ions in the plating solution is accomplished by the oxidation of the metal on the part being plated, rather than by a reducing agent in the solution. With immersion plating, therefore, the metal on the part is displaced—not coated—by metal ions in the solution and the process is self-limiting. When none of the original metal on the part remains in contact with the solution, the process stops. Only thin metal layers can be so plated, for example, for immersion gold, only a few microinches is possible.

Lamination: In printed wiring board manufacturing, lamination usually refers to the assembling of the layers of a multilayer panel in a press.

Land: A pad or land is the end of a circuit line or trace. A circuit feature designed to allow for component attachment (typically soldering), such as surface mount lands (usually rectangular) or lands surrounding plated through holes (usually circular). Typically, the pad or land is significantly wider than the rest of the circuit trace in order to approximately match the width of the component lead that will be attached to it.

Micro-etchant: In printed wiring board manufacturing, a chemical that oxidizes metallic copper. Micro-etchants remove 5 to 50 microinches of surface copper as a surface preparation or cleaning step.

MCM: Multichip Module. Multichip modules consist of multiple bare IC chips mounted directly on a substrate, often quite similar to a small printed wiring board. This MCM can then be coated for protec-

tion from moisture and other hazards and used as is or is mounted on another printed wiring board as part of a larger printed wiring assembly.

Multilayer: A circuit with more than two layers of interconnected circuitry. In addition to the top and bottom surface layers, one or more layers are embedded within the substrate.

OEM: Original Equipment Manufacturer. These companies manufacture printed wiring boards for use internally in their own electronic products.

Pad: A pad or land is the end of a circuit line or trace. A circuit feature designed to allow for component attachment (typically soldering), such as surface mount lands (usually rectangular) or lands surrounding plated through holes (usually circular). Typically, the pad or land is significantly wider than the rest of the circuit trace in order to approximately match the width of the component lead that will be attached to it.

Panel Plating: Term used to describe the copper plating of an entire printed wiring board panel. No mask or plating resist is applied.

Pattern Plating: Term used to describe the copper (or other metals) plating of a printed wiring board panel that has areas not included in the final circuit masked off with plating resist.

Pitch: Pitch refers to the distance from a point on a particular feature to the same point on the adjacent feature. Pitch, as used by the PWB industry, frequently defines the distance from the center of a circuit line (also called "trace") to the center of the adjacent line. The thinner the line and space (or finer the pitch), the more lines can be placed on the PWB.

Plated Through-Hole: A via or other drilled hole that is plated with copper. Since a printed wiring board substrate is not conductive (it consists of glass fibers and epoxy-resin), an electroless copper or other seed layer must be plated first before electrolytic copper can be applied. Copper is plated to a thickness of 0.001" on the walls of the hole, and this plating serves as a conductive pathway from layer to layer.

PWA: Printed Wiring Assembly. When electronic components have been mounted on the PWB, the combination of PWB and components is called a printed wiring assembly. This assembly is the basic building block for all larger electronic systems, from toys to toasters to telecommunications.

PWB: Printed Wiring Board, also called PCB for Printed Circuit Board.

Single-sided: A printed wiring board with only one layer of circuitry. Since no interconnection between layers is necessary, the electroless copper and other process steps are not necessary when manufacturing single-sided printed wiring boards.

Use Cluster: A use cluster is a set of chemicals, processes, and technologies that can substitute for one another to perform a specific function.

Via: Term used to describe holes drilled through a printed wiring board for the purposes of layer-to-layer interconnection. The conductive pathway between layers is completed by plating vias with copper. It is customary to refer to holes drilled only for the purposes interconnection as vias; other holes that may also provide interconnection but are also used for support of component leads or for tooling purposes are not generally called vias.