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ENVIRONMENTAL RESEARCH BRIEF

Waste Minimization Assessment for a Manufacturer of Silicon-Controlled Rectifiers and Schottky Rectifiers

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Abstract

The U.S. Environmental Protection Agency (EPA) has funded a pilot project to assist small- and medium-size manufacturers who want to minimize their generation of waste but who lack the expertise to do so. In an effort to assist these manufacturers Waste Minimization Assessment Centers (WMACs) were established at selected universities and procedures were adapted from the EPA *Waste Minimization Opportunity Assessment Manual* (EPA/625/7-88/003, July 1988). The WMAC team at Colorado State University performed an assessment at a plant manufacturing devices for converting alternating current into direct current (silicon-controlled rectifiers and Schottky rectifiers) — approximately 2.5 million units per year. Rectifier manufacture is a two step process: wafer fabrication and assembly. Silicon wafers are doped, spin coated, cleaned, and rinsed. Next, the wafers are etched and the resist is stripped to produce a final groove pattern. Layers of polysilicate and silicon nitride are deposited via chemical vapor deposition, silicon glass is fused to the surface ground, and then the wafer is cut into chips or dice. The dice are tested, sorted, and evaluated and then transferred to assembly. The team's report, detailing findings and recommendations, indicated that the majority of waste was generated by the stack scrubbers used to remove contaminants from exhausted plant air and that the greatest savings could be obtained by redirecting reject water from the reverse osmosis unit to the stack scrubbers to eliminate the wastewater stream from the reverse osmosis unit.

This Research Brief was developed by the principal investigators and EPA's Risk Reduction Engineering Laboratory, Cincinnati, OH, to announce key findings of an ongoing research project that is fully documented in a separate report of the same title available from University City Science Center

Introduction

The amount of waste generated by industrial plants has become an increasingly costly problem for manufacturers and an additional stress on the environment. One solution to the problem of waste is to reduce or eliminate the waste at its source.

University City Science Center (Philadelphia, PA) has begun a pilot project to assist small- and medium-size manufacturers who want to minimize their formation of waste but who lack the inhouse expertise to do so. Under agreement with EPA's Risk Reduction Engineering Laboratory, the Science Center has established three WMACs. This assessment was done by engineering faculty and students at Colorado State University's (Fort Collins) WMAC. The assessment teams have considerable direct experience with process operations in manufacturing plants and also have the knowledge and skills needed to minimize waste generation.

The waste minimization assessments are done for small- and medium-size manufacturers at no out-of-pocket cost to the client. To qualify for the assessment, each client must fall within Standard Industrial Classification Code 20-39, have gross annual sales not exceeding $75 million, employ no more than 500 persons, and lack inhouse expertise in waste minimization.

The potential benefits of the pilot project include minimization of the amount of waste generated by manufacturers, and reduction of waste treatment and disposal costs for participating plants. In addition, the project provides valuable experience for graduate and undergraduate students who participate in the program, and a cleaner environment without more regulations and higher costs for manufacturers.

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Methodology of Assessments

The waste minimization assessments require several site visits to each client served. In general, the WMACs follow the procedures outlined in the EPA *Waste Minimization Opportunity Assessment Manual* (EPA/625/7-88/003, July 1988). The WMAC staff locates the sources of waste in the plant and identifies the current disposal or treatment methods and their associated costs. They then identify and analyze a variety of ways to reduce or eliminate the waste. Specific measures to achieve that goal are recommended and the essential supporting technological and economic information is developed. Finally, a confidential report that details the WMAC's findings and recommendations (including cost savings, implementation costs, and payback times) is prepared for each client.

Plant Background

The plant produces silicon-controlled rectifiers (SCRs) and Schottky rectifiers for converting alternating current into direct current. The plant operates 2,100 hr/yr to produce approximately 2.5 million units.

Manufacturing Process

The raw materials used by the plant include 4-in. silicon wafers, various metals, photolithographic chemicals, photoresist, nitric acid, sulfuric acid, hydrochloric acid, silicon glass, resist stripper, plating chemicals, solder, and isopropyl alcohol.

The following steps are involved in making the various rectifiers:

Wafer Fabrication

Fabrication of individual electronic chips varies slightly for each of the two main products. In both cases, 4-in. silicon wafers purchased from an external supplier are used as the substrates. The wafer fabrication process generates p-n junctions and circuitry for chips that are cut from the wafers. As many as 200 chips can be fabricated from each wafer.

Chips for SCRs are manufactured in a clean room. During the initial production steps prior to clean-room processing, the wafers are doped with boron, phosphorus, and other metals. This process involves heating in electrical induction furnaces to temperatures above 600 °C for 18 hr. The doped wafers are then transported to the clean room. Photolithographic processes are used in the clean room to generate a pattern of grooves for each chip. The grooves extend into about 40% of the wafer thickness and expose the electrically active portion of the substrate. Negative-image liquid photoresist is applied to the doped wafers by an automated spin coating machine. A photomask is then placed over the wafer, and the resist is exposed to UV radiation to polymerize the resist and generate the groove pattern for each chip. The wafer is then developed and etched with nitric, sulfuric, and hydrochloric acids to remove unwanted material. The specific acids used depend on the product being manufactured. The resist is then removed by placing the wafer in a tunnel oven at 480 °C to char the resist. Residual material is removed with compressed air. The processes of resist coating, exposure, etching, and resist stripping may be repeated several times, depending upon the product being manufactured. When the final groove pattern is completed, layers of polysilicate and silicon nitride are deposited onto the wafer surfaces by chemical vapor deposition. Preformed silicon glass is applied and fused to the wafers to provide glass passivation. The wafers are then coated with metal, scribed with a laser, and divided into individual chips or dice. The dice are then tested, sorted, evaluated, and stored prior to assembly.

In addition to the advanced processes used to fabricate chips in the clean rooms, about 5% of the chips are manufactured using traditional wet chemistry electroplating techniques to deposit and etch metals. These techniques are used for certain SCRs. The wet chemistry consists of electroless nickel plating of the silicon wafer, acid etch, nickel plating, and gold plating. Roofing tar is used as the plating resist. Passivation of the silicon surface is accomplished with a potassium hydroxide solution. When the process is complete, the wafers are scribed with a laser, divided into dice, and sorted prior to assembly. Dice testing must be performed after assembly.

Fabrication of Schottky rectifiers is also performed in a clean room. The wafers are first cleaned and surface-oxidized. Spin coating and photolithographic processes similar to those used for SCRs provide a patterned mask on the wafer surface. Boron is then diffused onto the surface with high temperature induction furnaces. The resist is then removed with a phenol-based liquid resist stripper. Other mask/etch/deposition/resist strip processes follow for various elements required to build the desired patterns for the Schottky circuitry. After the final patterns have been deposited, the front sides of the wafers are coated with a protective layer of photoresist and a circular adhesive dot. The wafers are then removed from the clean room in semi-sealed containers to a grinding room where the back sides of the wafers are ground with porous ceramic abrasive to remove about 10 mils. The wafers are transported back to the clean room, where the adhesive dot and the photoresist are removed and the back sides of the wafers are coated with metal and cleaned. Completed wafers are transported from the clean room to a wafer saw with a diamond-tipped blade. The saw cuts the wafers into individual dice which are then tested and stored prior to assembly.

Assembly

Initial assembly procedures involve fusing the die into a pellet in a process called solder mountdown. A pellet consists of layered components that begin with a preformed disk of solder brazed onto a nickel-plated copper or steel stud, a molybdenum disk, another solder preform, and a die. The pellet is assembled by hand and placed in one of several tunnel ovens to fuse the components together. The ovens use a 100% hydrogen atmosphere, with nitrogen blankets at the entrances and exits to prevent oxidation. Fusing seals the mounted pellet to prevent arcing with RTV, a white caulk-like material that vulcanizes at room temperature. External packaging is welded onto the pellet/stud assembly and then the top ends of the rectifiers are crimped to seal off holes. Some devices require a solderable top. These units are dipped in flux and in a molten solder pot and then rinsed in alcohol. Automated and manual testing is performed on the final products before packaging, storage, and shipment to customers.

An abbreviated process flow diagram is shown in Figure 1.

Existing Waste Management Practices

This plant has already implemented the following techniques to manage and minimize its wastes.

- High-purity waste solvents from wafer fabrication are re-used in the assembly area before disposal.

- The potassium hydroxide passivation process has been eliminated since the initial visit by the WMAC team. The result of this action is that methanol use and disposal have been reduced 50%.
- Recent changes in material specifications have resulted in the elimination of an oil coating on the copper and steel studs received for assembly. 1,1,1-trichloroethane (TCA) used onsite to remove this oil has therefore been eliminated.

Waste Minimization Opportunities

The type of waste currently generated by the plant, the source of the waste, the quantity of the waste, and the treatment and disposal costs are given in Table 1.

Table 2 shows the opportunities for waste minimization that the WMAC team recommended for the plant. The type of waste, the minimization opportunity, the possible waste reduction and associated savings, and the implementation cost along with the payback time are given in the table. The quantities of waste currently generated by the plant and possible waste reduction depend on the production level of the plant. All values should be considered in that context.

It should be noted that, in most cases, the economic savings of the minimization opportunities result from the need for less raw material and from reduced present and future costs associated with waste treatment and disposal. Other savings not quantifiable by this study include a wide variety of possible future costs related to changing emissions standards, liability, and employee health. It should also be noted that the savings given for each opportunity reflect the savings achievable when implementing each waste minimization opportunity independently and do not reflect duplication of savings that would result when the opportunities are implemented in a package.

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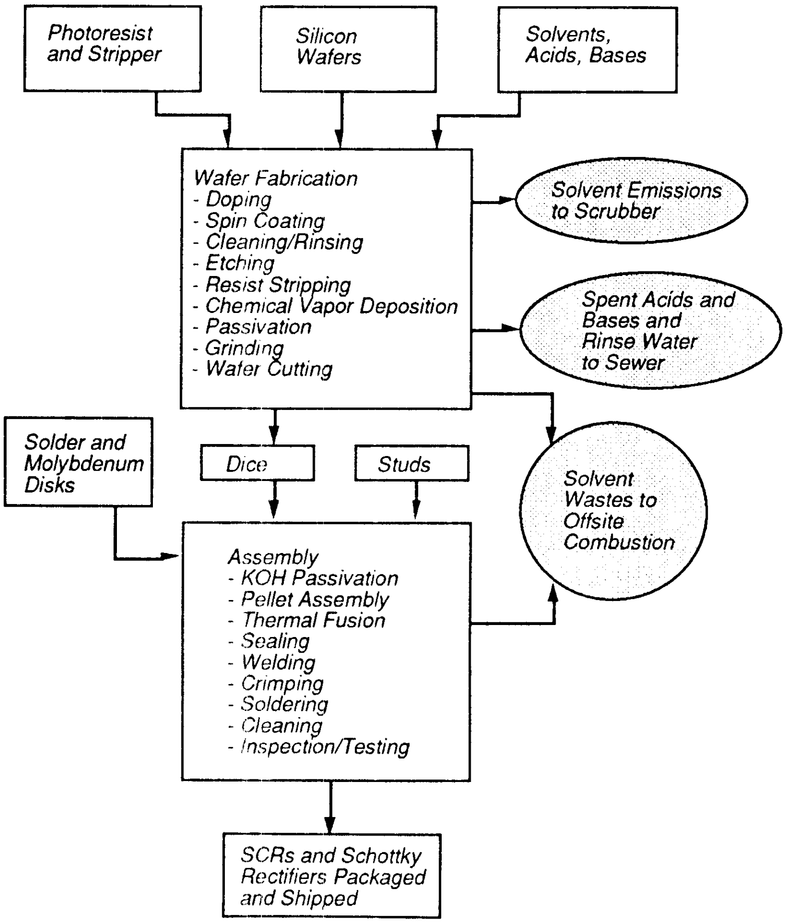

Figure 1. Abbreviated process flow diagram.

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Table 1. Summary of Current Waste Generation

Waste Generated	Source of Waste	Annual Quantity Generated (gal)	Annual Waste Management Cost [1]
Resist stripper	Wafer fabrication process for Schottky rectifiers	730	$13,630
Xylene	Removal of residual resist stripper from the wafers following stripping	1,795	12,450
Acetone	Removal of the protective adhesive dot and photoresist coating from the wafers after grinding	620	5,160
Mixed solvent wastes including n-butyl acetate, xylene, and spent photoresist waste	Removal of excess photoresist from the wafers in the spin coating equipment	420	7,120
Isopropyl alcohol	Removal of xylene from the wafers	315	3,570
Waste acids and bases including ammonium hydroxide, hydrogen peroxide, sulfuric acid, hydrochloric acid, hydrofluoric acid, and nitric acid	Etching and cleaning between process steps	11,618	71,360
Rinse water	Wafer fabrication	1,908,816	27,130
Methyl alcohol	Cleaning and drying	2,295	11,220
1,1,1-Trichloroethane	Ultrasonic degreaser and vapor degreaser	840	7,980
Freon	Vapor degreaser	55	14,620
Stack scrubber water	Scrubber system	4,032,000	14,860
Reverse osmosis reject water	Reverse osmosis unit	818,064	3,850

[1] Includes raw material costs

Table 2. Summary of Recommended Waste Minimization Opportunities

Waste Generated	Minimization Opportunity	Annual Waste Reduction		Net Annual Savings	Implementation Costs	Payback Years
		Quantity	Percent			
RO reject water	Reuse reject water from the reverse osmosis unit for use in the stack scrubber system.	818,064 gal	100	$2,142	$5,111	2.4
Resist strip	Replace resist strip with a water miscible, biodegradable, nontoxic product containing no aromatic hydrocarbons. This product will be used with a supplemental stripper rinse solution.	730 gal	100	1,184	0	immediate
Isopropyl alcohol		300 gal	100			
Xylene		200 gal	100			
1,1,1-Trichloroethane	Replace 1,1,1-trichloroethane vapor degreasing with a nontoxic, nonhazardous, low volatility aqueous cleaner and cleaner rinse.	55 gal	100	604	1,550	2.6

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